

2019 IEEE VTS

April 23-25, 2019
MONTEREY(CA), USA



TEST RELIABILITY AND SECURITY CHALLENGES IN VLSI SYSTEMS

CALL FOR PAPERS

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in testing, reliability and security of microelectronic circuits and systems. The VTS Program Committee invites original, unpublished **paper submissions** for VTS 2019. Proposals for the **innovative practices** and **special sessions tracks** are also invited.

Program Committee:

J. Abraham – University of Texas at Austin
V. Agrawal – Auburn University
C. Argyrides – AMD
M. Barragan – TIMA Laboratory
B. Becker – Universität Freiburg
R. Blanton – Carnegie Mellon University
A. Bosio – INL – Ecole Centrale de Lyon
K. Chakrabarty – Duke University
T. Chakrabarty – Independent
A. Chatterjee – Georgia Tech
D. Chen – Iowa State University
H. Chen – Mediatek
K. Chung – Qualcomm
J. Colburn – Nvidia
W. Dobbelaere – ON Semiconductor
D. Gizopoulos – University of Athens
S. Gupta – USC
S. Hellebrand – University of Paderborn
Y. Huang – Mentor Graphics
E. Larsson – Lund University
H. Li – Chinese Academy of Sciences
T.M. Mak – Independent
H. Manhaeve – Ridgetop
M. Maniatakos – NYU-AD
P. Maxwell – ON Semiconductor
S. Mir – TIMA Laboratory
Z. Navabi – WPI
A. Orailoglu – UCSD
I. Pomeranz – Purdue University
J. Rajski – Mentor Graphics
S. Reddy – University of Iowa
M. Ricchetti – Synopsys
E. Sanchez – Politecnico di Torino
S. Shoukourian – Synopsys
O. Sinanoglu – NYU Abu Dhabi
H. Stratigopoulos – LIP6
S. Sunter – Mentor Graphics
M. Tehranipoor – University of Florida
C. Thibeault – ETS Montreal
L. C. Wang – UCSB
H.J. Wunderlich – University of Stuttgart

Major topics include but are not limited to:

Analog/Mixed-Signal/RF Test
ATPG & Compression
Silicon Debug
Automotive Test & Safety
Built-In Self-Test (BIST)
Defect & Current Based Test
Defect/Fault Tolerance
Delay & Performance Test
Design for Testability (DFT)
Design Verification/Validation

Embedded System & Board Test
Embedded Test Methods
Emerging Technologies Test
FPGA Test
Fault Modeling and Simulation
Hardware Security
Low-Power IC Test
Microsystems/MEMS/Sensors Test
Memory Test and Repair
On-Line Test & Error Correction

Power/Thermal Issues in Test
System-on-Chip (SOC) Test
Test Standards
Test Economics
Test of Biomedical Devices
Test of High-Speed I/O
Test Quality and Reliability
Test Resource Partitioning
Transients and Soft Errors
2.5D, 3D and SiP Test

New hot topics:

*This year VTS puts particular emphasis on enlarging its scope soliciting submissions on testing, reliability and security aspects on the following hot topics: **approximate computing, neuromorphic computing and quantum computing***

KEY DATES

Oct 19, 2018 (EXTENDED) - Title registration
Oct 26, 2018 (EXTENDED) - PDF upload
Dec 09, 2018 - Notifications
Feb 10, 2019 - Camera ready upload

Submissions

6 pages in a standard IEEE
two columns format.

Submit at:
<http://www.tttc-vts.org>

VTS 2019 will present a Best Paper Award, a Best Special Session Award, and a Best Innovative Practices Session Award based on the evaluations of reviewers, attendees, and an invited panel of judges. We also plan to organize various Student Activities including the TTTC Best Doctoral Thesis Contest, details for which will be made available through the VTS website.

VTS 2019 will have a Special Issue on IEEE Transactions on Emerging Topics. A selection of the best papers will be invited to submit an extended version to IEEE Transactions on Emerging Topics.

TTTC Test Technology Educational Program (TTEP) tutorials on emerging test technology topics will be offered in conjunction with VTS 2019. Tutorial proposals should be submitted according to TTEP 2019 submission guidelines, which will be posted on <http://computer.org/tab/tttc/teg/ttep>.

Organizing Committee:

General Chair: Chen-Huan Chiang – Intel Inc.
Vice-General Co-Chairs: L. Anghel – TIMA Laboratory
Past Chair: Y. Makris – UT Dallas Montreal
Program Co-Chairs: S. Di Carlo – P. di Torino
P. Song – IBM Research
Vice-Program Co-Chairs: M. Tahoori – Karlsruhe Inst. of Tech.
S. Ozev – Arizona State University
Innovative Practices Co-Chairs: P. Sarson – Dialog Semiconductor
J. Carulli – Globalfoundries
Special Sessions Co-Chairs: J. Dworak – Southern Methodist U.
M. Michael – University of Cyprus
I. Vatajelu (Chair) – TIMA Laboratory
G. Di Natale (Member) – LIRMM
Publications: A. Savino – Politecnico di Torino
Publicity Chair: H. Kobayashi – Gunma University
Asian Initiative Chair:

Steering Committee:

M. Abadir – Abadir & Associates
J. Figueras – UPC
A. Ivanov – U. of British Columbia
M. Nicolaidis – TIMA Laboratory
P. Prinetto – Politecnico di Torino
A. Singh – Auburn University
P. Varma – Real Intent
Y. Zorian – Synopsys

General Chair



Chen-Huan Chiang
Intel Inc.
chen-huan.chiang@intel.com

Program Co-Chairs

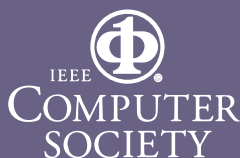


Peilin Song
IBM Research
psong@us.ibm.com



Stefano Di Carlo
Politecnico di Torino
stefano.dicarlo@polito.it

Sponsored by



For information, visit
www.tttc-vts.org