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31st IEEE VLSI TEST SYMPOSIUM The Claremont, Berkeley, CA, USA April 29 - May 2, 2013

Preliminary Call for Papers

The IEEE VLSI Test Symposium (VTS) explores emerging trends and novel concepts in testing, debug and repair of microelectronic circuits and systems. Major topics include, but are not limited to:

- Analog, Mixed-Signal & RF Test Embedded System & Board Test
 - ATPG & Compression
- ATE Architecture & Software
- Built-In Self-Test (BIST)
- Defect & Current Based Test
- Defect/Fault Tolerance
- Delay & Performance Test
- Design for Testability (DFT)
 - Design Verification/Validation
- Diagnosis and Debug
- Embedded Test Methods **Emerging Technologies Test**
- FPGA Test
- Fault Modeling and Simulation
- Hardware Security
- Memory Test and Repair
- System-on-Chip (SOC) Test

- The VTS Program Committee invites original, unpublished paper submissions for VTS 2013. Paper submissions should be complete manuscripts, up to six pages (inclusive of figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, and e-mail address of the contact author. A 50-word abstract and five keywords identifying the topic area are also required.

Proposals for the Innovative Practices and Special Sessions tracks are also invited. The innovative practices track highlights cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. Special sessions can include panels, embedded tutorials, or hot topic presentations. Innovative practices and special session track proposals should include a title, name and contact information of the session organizer(s), a 150-to-200 word abstract, and a list of prospective participants.

All submissions are to be made electronically through the VTS website. The deadline for all submissions is October 19th 2012. Detailed instructions for submissions are to be found at the symposium website http://www.tttc-vts.org. Authors will be notified of the disposition of their papers by December 21st, 2012. A submission will be considered as commitment that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the symposium proceedings and will present the paper at the symposium. The registration of at least one author is required for publication. The organizing committee of VTS reserves the right to exclude a paper from distribution after the symposium (e.g., removal from IEEE Xplore) if the paper is not presented at the symposium. In the case of innovative practices and special sessions, the organizers commit to submitting a session title, abstract, and a list of participants for inclusion in the symposium proceedings.

VTS 2013 will present a Best Paper Award, a Best Special Session Award, and a Best Innovative Practices Session Award based on the evaluations of reviewers, attendees, and an invited panel of judges. We also plan to organize a Student Poster Competition and a TTTC Best Doctoral Thesis Contest, details for which will be available through the VTS website at a later date. The best paper of VTS 2013 and the best Innovative Practices presentation will be invited to resubmit to the IEEE Design & Test of Computers and will undergo the regular, but expedited, review process of this periodical.

TTTC Test Technology Educational Program (TTEP) tutorials on emerging test technology topics will be offered in conjunction with VTS 2013. Tutorial proposals should be submitted according to TTEP 2013 submission deadlines, which will be posted on http://computer.org/tab/tttc/teg/ttep.

VTS 2013 is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society. For more information on the symposium, please visit the VTS website at http://www.tttc-vts.org or contact:

For general information: **GENERAL CHAIR** Michel Renovell LIRMM - University of Montpellier renovell@lirmm.fr

For submission related information: **PROGRAM CHAIR Yiorgos Makris** The University of Texas at Dallas viorgos.makris@utdallas.edu





- Low-Power IC Test Microsystems, MEMS and Sensor Test
 - - **On-Line Test & Error Correction**
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Test Economics

- Test of Biomedical Devices
- Test of High-Speed I/O
- Test Quality and Reliability
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- 2.5D, 3D and SiP Test