28th IEEE VLSI TEST SYMPOSIUM

Preliminary Call for Papers

Santa Cruz, California, USA

New Date: April 18 – 21, 2010

The **IEEE VLSI Test Symposium** (VTS) explores emerging trends and novel concepts in testing, and verification / validation of microelectronic circuits and systems. Major topics include, but are not limited to:

- *Analog, Mixed-Signal & RF Test*
- *ATPG & Compression*
- *ATE Architecture & Software*
- *Board & System Test*
- *Built-In Self-Test (BIST)*
- *Current Based Test*
- *Defect/Fault Tolerance & Self-Repair*
- *Delay & Performance Test*
- *Design for Testability (DFT)*
- *Design Verification/Validation*
- *Diagnosis and Debug*
- *Embedded System and Microsystems Test*
- *Embedded Test Methods*
- *FPGA Test*
- *Fault Modeling and Simulation*
- *Infrastructure IP*
- *Low-Power IC Test*
- *MEMS and Sensor Test*
- *Memory Test and Repair*
- *Emerging Technologies Test*
- *On-Line Test*
- *Power Issues in Test*
- *System-on-Chip (SOC) Test*
- *System-in-Package Test*
- *Standards*
- *Test Economics*
- *Thermal Test*
- *Test of Biomedical Devices*
- *Test of High-Speed I/O*
- *Test Quality and Reliability*
- *Test Resource Partitioning*
- *Transients and Soft Errors*

The VTS Program Committee invites **original, unpublished paper submissions** for VTS 2010**.** Paper submissions should be complete manuscripts, up to six pages (inclusive of figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. A 50-word abstract and five keywords identifying the topic area are also required.

Proposals for the **Innovative Practices track,** and **Special Sessions** are also invited**.** The innovative practices track will highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. Special sessions can include panels, embedded tutorials, or hot topic presentations. Innovative practices track and special session proposals should include a title, name and contact information of the session organizer(s), a 150-to-200 word abstract, and a list of prospective participants.

All submissions are to be made electronically through the VTS website. The deadline for all submissions is **September 20th 2009**. Detailed instructions for submissions are to be found at the conference website **http://www.tttc-vts.org.** Authors will be notified of the disposition of their papers by January 8th 2010. A submission will be considered as evidence that, upon acceptance, the author(s) will submit a final camera-ready version of the paper for inclusion in the proceedings, and will present the paper at the symposium. The registration of at least one author is required for publication. In the case of innovative practice and special sessions, the organizers commit to submit a session title, abstract, and list of participants for inclusion in the symposium proceedings and program.

VTS 2010 will present a **Best Paper Award**, a **Best Panel Award**, and a **Best IP Track Session Award** based on the evaluations of reviewers, attendees, and an invited panel of judges. We also plan to organize a **Student Poster Competition** and a **TTTC Best Doctoral Thesis Contest**, details will be available later.

TTTC Test Technology Educational Program (TTEP) tutorials on emerging test technology topics will be offered during VTS 2010. Tutorial proposals should be submitted according to TTEP 2010 submission deadlines (http://computer.org/tab/tttc/teg/ttep).

VTS 2010 is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society. For more information on the VTS 2010 Test Event, visit the VTS website at ***http://www.tttc-vts.org*** or contact**:**

For general information:

GENERAL CHAIR

Magdy Abadir

Freescale

m.abadir@freescale.com

For submission related information:

PROGRAM CO-CHAIRS

Michel Renovell

LIRMM-CNRS

renovell@lirmm.fr

Claude Thibeault

École de technologie supérieure

claude.thibeault@etsmtl.ca

IMPORTANT : PAPER SUBMISSION DEADLINE ON SEPT 20th

IEEE VLSI Test Symposium
1474 Freeman Drive
Amissville, VA 20106, USA
Tel: +1-540-937-8280 Fax: +1-540-937-7848
Email: tttc@computer.org