28th IEEE VLSI TEST SYMPOSIUM (VTS 2010)
Seascape Beach Resort, Santa Cruz California, USA
April 19th – April 22nd, 2010
http://www.tttc-vts.org

Call for Participation

The IEEE VLSI Test Symposium explores emerging trends and novel concepts in the testing of integrated circuits and systems. The symposium is a leading international forum where many of the world's leading test experts and professionals from both industry and academia join to present and debate key issues in testing. VTS 2010 addresses key trends and challenges in the semiconductor design and manufacturing industries through an exciting program that includes Keynote and Plenary Talks, Technical Paper Sessions, Panels, New Topic Sessions, Full-day Tutorials, co-located Workshops, and the Innovative Practices Track.

TECHNICAL PAPER SESSIONS will present the latest research results in test, including:

- Analog/Mixed-Signal Test
- ATPG and Compression
- Delay and Performance Test
- Low-power IC Test
- Memory Test and Repair
- NBTI and Early Life Failures
- On-line and System Testing
- RF Test
- Test for Emerging Technologies
- Test Optimizations
- Transient and Soft Errors
- Yield Modeling and Defects

EMBEDDED TUTORIAL

Test and Fault Tolerance of Networks-on-Chip

INNOVATIVE PRACTICES (IP) TRACK highlights:

- Practices in RF Test
- Industrial Practices for Test Cost Reduction
- Verification and Testing Challenges in High-Level Synthesis
- Implications of Power Delivery Network for Validation and Testing
- Post-Silicon Debug
- 3D Chip Testing

FEATURED PANELS:

- Adaptive Analog Test
- Apprentice – VTS Edition: Season 3;
- Low-Power Test and Noise-Aware Test
- EDA for Analog DFT/ATPG

HOT TOPIC SESSIONS

- Design Consideration and Silicon Evaluation of On-Chip Monitors
- MOS/MTJ-Hybrid Circuit with Nonvolatile Logic-in-Memory Architecture and Its Impact
- Mixed-Signal Test Impact to SoC Commercialization
- 3-D Testing
- Test Facilities and Infrastructure in Canada
- Hardware Security: Test and Verification Issues

OTHER SESSIONS

- Thesis Research Posters
- E.J. McCluskey Doctoral Thesis Competition

One WORKSHOP and two TUTORIALS complement the core technical program of VTS.

WORKSHOP

- IEEE Workshop on Test of Wireless Circuits and Systems (WTW)

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) Full-day TUTORIALS

- Practices in Analog, Mixed-signal and RF Testing.
- Parameter Variations and Low-power Design: Test Issues & On-chip Calibration/Repair Solutions

Social Activities: VTS provides an opportunity for informal technical discussions among participants. This year, the social program will feature a visit to a local attraction (transportation provided) and a banquet sunset dinner on the beach. Attendees will also receive complementary breakfast, lunch and breaks each day of the conference. Santa Cruz, California provides a very attractive backdrop for all VTS 2010 activities. We are sure that you will find VTS 2010 enlightening, thought-provoking, rewarding, and enjoyable!

Sponsor and Corporate Support: VTS 2010 is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society. VTS also has several corporate supporters. Please visit the VTS website for full details (*http://www.tttc-vts.org*).

For a Preliminary Program, Conference Registration and Hotel Information please visit (*http://www.tttc-vts.org*).

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