28th IEEE VLSI Test Symposium (VTS 2010)
Santa Cruz, CA, April 19-21, 2010

Preliminary Program (as of 4/18/10)

Monday, 4/19/10

Plenary Session (9:00 – 11:00)

Welcome Message:
Magdy Abadir, General Chair

Program Introduction:
Michel Renovell and Claude Thibeault, Program Co-Chairs

Keynote Speaker:
Robert Madge, Director of Technology, LSI Logic

Invited Keynote:
Ron Collett, CEO & President, Nemetrics

Awards presentation:
IEEE Fellow Awards
TTTC Most Successful Technical Meeting Award
TTTC Most Populous Technical Meeting Award
VTS 2009 Best Paper Award
VTS 2009 Best Panel Award
VTS 2009 Best Innovative Practices Award

Break (11:00 – 11:15)

Sessions 1 (11:15 – 12:15)

Session 1A: Delay & Performance Test 1
Moderator: M. Batek - Broadcom
Fast Path Selection for Testing of Small Delay Defects Considering Path Correlations
Z. He, T. Lv - Institute of Computing Technology, H. Li, X. Li - Chinese Academy of Sciences
Identification of Critical Primitive Path Delay Faults without any Path Enumeration
K. Christou, M. Michael, S. Neophytou - University of Cyprus
Path Clustering for Adaptive Test
T. Uezono, T. Takahashi - Tokyo Institute of Technology, M. Shintani , K. Hatayama - Semiconductor Technology Academic Research Center, K. Masu - Tokyo Institute of Technology, H. Ochi, T. Sato - Kyoto University

Session 1B: Memory Test & Repair
Moderator: P. Prinetto - Politecnico di Torino
Automatic Generation of Memory Built-In Self-Repair Circuits in SOCs for Minimizing Test Time and Area Cost
T. Tseng, C. Hou, J. Li - National Central University

Bit Line Coupling Memory Tests for Single Cell Fails in SRAMs
S. Irobi, Z. Al-ars, S. Hamdioui - Delft University of Technology
Reducing Test Time and Area Overhead of an Embedded Memory Array Built-In Repair Analyzer with Optimal Repair Rate
J. Chung, J. Park - The University of Texas at Austin, E. Byun, C. Woo - Samsung Electronics, J. Abraham - The University of Texas at Austin

IP Session 1C: Innovative Practices in RF Test
Organizer: R. Parekhji - Texas Instruments
Moderator: K. Arnold - Pintail
Test Time Reduction Using Parallel RF Test Techniques
R. Mittal, A. Sontakke, R. Parekhji, Texas Instruments, Bangalore
Density Estimation for Analog/RF Test Problem Solving
S. Mir, H. Stratigopoulos -TIMA, A. Bounceur - European University of Brittany
Low Cost Test and Tuning of RF Circuits and Systems
F. Taenzler - Texas Instruments, A. Chatterjee - Georgia Institute of Technology

Lunch (12:15 – 13:30)

Sessions 2 (13:30 – 14:30)

Session 2A: Delay & Performance Test 2
Moderator: F. Ferhani - Broadcom
A Novel Hybrid Method for SDD Pattern Grading and Selection
K. Peng, J. Thibodeau - University of Connecticut, M. Yilmaz - AMD, K. Chakrabarty - Duke University, M. Tehranipoor - University of Connecticut
Forming Multi-Cycle Tests for Delay Faults by Concatenating Broadside Tests
I. Pomeranz - Purdue University, S. Reddy - University of Iowa
An Output Compression Scheme for Handling X-states from Over-Clocked Delay Tests
A. Singh, C. Han, X. Quian - Auburn University

Session 2B: Dealing with NBTI and Gate-Oxide Early Life Failure
Moderator: L. Winemberg - Freescale
Reliable Cache Design with On-Chip Monitoring of NBTI Degradation in SRAM Cells using BIST
F. Ahmed, L. Milor - Georgia Institute of Technology
Gate-Oxide Early Life Failure Identification using Delay Shifts
Y. Kim, T. Chen - Stanford University, Y. Kameda, M. Mizuno - NEC Corporation, S. Mitra - Stanford University
Detecting NBTI Induced Failures in SRAM Core-Cells
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Virazel - LIRMM, N. Badereddine - Infineon

IP Session 2C: Design, Fabrication, and Test of Flexible Electronics
Organizer: K. Cheng - UC Santa Barbara
Moderator: B. Kaminska – Simon Fraser U.
Design, Analysis, and Test of Low-Power and Reliable Flexible Electronics
K. Cheng, T. Huang - UC Santa Barbara
Fabrication and Testing of Large-area Flexible Electronics for Displays and Sensor Arrays
W. Wong - Palo Alto Research Center
Overview of Flexible Electronics from ITRI's Viewpoint
J. Hu - ITRI

Break (14:30 – 14:45)

Sessions 3 (14:45 – 15:45)

Session 3A: Delay & Performance Test 3

Moderator: B. Becker - University of Freiburg

Impact of Multiple Input Switching on Delay Test under Process Variation

S. Wu – UC Santa Barbara, S. Chakravarty - LSI, L. Wang - UC Santa Barbara

Low-Power Test Planning for Arbitrary At-Speed Delay-Test Clock Schemes

C. Zoellin, H. Wunderlich - Universität Stuttgart

Selecting the Most Relevant Structural Fmax for System Fmax Correlation

J. Chen – UC Santa Barbara, J. Zeng - Advanced Micro Devices, L. Wang - UC Santa Barbara

Session 3B: Emerging Technologies Test

Moderator: S. Davidson - Oracle

On-the-fly Variation Tolerant Mapping in Crossbar Nano-Architectures

M. Tahoori, C. Tunc - Northeastern University

Pin-Count-Aware Online Testing of Digital Microfluidic Biochips

Y. Zhao, K. Chakrabarty - Duke University

iMajik: Making 1149.1 TAPs Disappear and Reappear in SoCs and 3D Packages

C. Clark - Intellitech Corporation

IP Session 3C: Industrial Practices of Test Cost Reduction Techniques: Impact and Design Tradeoffs

Organizer: S. Tammali - Texas Instruments Inc.

Moderator: Phil Nigh, IBM

Industrial Practices of Test Cost Reduction: Perspective, Current design practices

S. Tammali, Q. Qin - Texas Instruments Inc.

Adaptive Test Delivers Wide Range of Sophisticate Test Solutions

K. Arnold - Pintail Technologies

Test Cost and Test Power Conflicts: EDA Perspective

M. Hirech - Synopsys

Break (15:45 – 16:00)

Sessions 4 (16:00 – 17:30)

Special Session 4A: Apprentice - VTS Edition: Season 3

Organizer/Moderator: K. S. Kim - Samsung

Special Session 4B: Panel: Low-Power Test and Noise-Aware Test: Foes or Friends?

Organizer: I. Polian - University of Freiburg

Moderator: S. Reddy - University of Iowa

Panelists: W. Cheng - Mentor Graphics

S. Chakravarty - LSI

M. Zhang - Intel

X. Wen - KIT

Y. Zorian - Virage Logic

Special Session 4C: Thesis Research Posters

Organizer: H. Stratigopoulos - TIMA Lab

Moderator: P. Bernardi - Politecnico di Torino

Tuesday, 4/20/10

Sessions 5 (8:00 – 9:00)

Session 5A: Low-Power IC Test

Moderator: M. Tehranipoor - University of Connecticut

A Generic Low Power Scan Chain Wrapper for Designs Using Scan Compression

A. Sabne – Bhel, R. Tiwari, A. Shrivastava, S. Ravi, R. Parekhji - Texas Instruments

Low-Capture-Power At-Speed Testing using Partial Launch-on-Capture Test Scheme

Z. Chen, D. Xiang - Tsinghua University

Theoretical Analysis for Low-Power Test Decompression Using Test-Slice Duplication

S. Mu, M. Chao - National Chiao-tung University

Session 5B: Transients & Soft Errors

Moderator: M. Zang - Intel

CSER: BISER-Based Concurrent Soft-Error Resilience

L. Wang - Syntest Technologies, Inc., N. Touba - University of Texas at Austin, Z. Jiang, S. Wu - Syntest Technologies, Inc., J. Huang, J. Li - National Taiwan University

Workload-Driven Selective Hardening of Control State Elements in Modern Microprocessors

M. Maniatakos, Y. Makris - Yale University

Scalable and Accurate Estimation of Probabilistic Behavior in Sequential Circuits

C. Yu, J. Hayes - University of Michigan

IP Session 5C: Post-Silicon Debug

Organizer: S. Gupta - USC

Moderator: T. Ziaja - Oracle

Post-silicon debug leveraging embedded memory based solutions

G. Torjyan, Y. Zorian - Virage Logic

Beyond design... Productizing IA silicon

K. Tiruvallur - Intel Corp.

Presentation 3 - TBA

Presenter 3 - Affiliation

Break (9:00 – 9:15)

Sessions 6 (9:15 – 10:15)

Session 6A: Power Issues in Test

Moderator: H. Wunderlich - University of Stuttgart

At-Speed Scan Test with Low Switching Activity

E. Moghaddam - University of Iowa , J. Rajski - Mentor Graphics, S. Reddy - University of Iowa, M. Kassab - Mentor Graphics

Low-Power Compression Architecture

S. Bhatia - Atrenta

Thermal-Uniformity-Aware X-Filling to Reduce Temperature-Induced Delay Variation for Accurate At-Speed Testing

T. Yoneda, M. Inoue - Nara Institute of Science and Technology, Y. Sato - Kyusyu Institute of Technology, H. Fujiwara - Nara Institute of Science and Technology

Session 6B: Yield Modeling & Defects

Moderator: H. Manhaeve - Q-StarTest

Modeling Yield, Cost, and Quality of an NoC with Uniformly and Non-Uniformly Distributed Redundancy

S. Shamshiri, K. Cheng - UC Santa Barbara

Evaluating Yield and Testing Impact of Sub-Wavelength Lithography

W. Tam , R. Blanton , W. Maly - Carnegie Mellon University
Defect Diagnosis Based on DFM Guidelines
D. Kim,, I. Pomeranz - Purdue University, M. Amyeen , S. Venkataraman - Intel Corporation

Special Session 6C: New Topic
Organizer: B. Kaminska - Simon Fraser University
Moderator: S. Sunter - Mentor Graphics
Mixed-Signal Test Impact to SoC Commercialization
K.Arabi - Qualcomm

Break (10:15 – 10:30)

Sessions 7 (10:30 – 11:30)

Session 7A: ATPG & Compression
Moderator: S. Hellebrand – University of Paderborn
Application of Signal and Noise Theory to Digital VLSI Testing
N. Yogi , V. Agrawal - Auburn University
On Multiple Bridging Faults
I. Pomeranz - Purdue University, S. Reddy - University Of Iowa
Reusing NoC-Infrastructure for Test Data Compression
V. Froese , R. Ibers, S. Hellebrand - University Of Paderborn

Session 7B: On-line & System Testing
Moderator: A. Orailoglu - UC San Diego
Concurrent Autonomous Self-Test for Uncore Components in System-on-Chips
Y. Li - Stanford University, O. Mutlu - Carnegie Mellon University, D. Gardner - Intel Labs, S. Mitra - Stanford University
Low-sensitivity to Process Variations Aging Sensor for Automotive Safety-Critical Applications
J. Vazquez, V. Champac - Istituto Nacional de Astrofisica, A. Ziesemer Jr., R. Reis -UFRGS, I. Teixeira, M. Santos, J. Teixeira - Lisboa Technical University
Board-level Fault Diagnosis using Bayesian Inference
Z. Zhang, Z. Wang - Duke University, X. Gu - Cisco Systems, Inc., K. Chakrabarty - Duke University

IP Session 7C: Verification and Testing Challenges in High-Level Synthesis
Organizers: S. Ray - University of Texas at Austin, J. Bhadra - Freescale Semiconductor
Moderator: J. Bhadra - Freescale Semiconductor
The Roadblocks to Broad Adoption of High Level Synthesis
M. Keating - Synopsys Inc.
High Level Synthesis of a Front End Filter and DSP Engine for Analog to Digital Conversion - A Case Study
J. Mena, R. Deken, J. Coker, M. Johnstone - Freescale Semiconductor, Inc., Sergio R. Ramirez, Peter Frey - Cadence Design Systems
Easing the Verification Bottleneck using High-level Synthesis
D. Varma, D. Mackay, P. Thiruchelvam - AutoESL Design Technologies

Sessions 8 (12:45 – 14:15)

Special Session 8A: E.J. McCluskey Doctoral Thesis Competition
Organizer: H. Stratigopoulos - TIMA Lab
Moderator: P. Bernardi - Politecnico di Torino

Special Session 8B: New Topic
Organizer: B. Courtois - CMP

Moderator: L. Anghel – TIMA Lab.
MOS/MTJ-Hybrid Circuit with Nonvolatile Logic-in-Memory Architecture and Its Impact
T. Hanyu - Tohoku University

Special Session 8C: Panel: EDA for Analog DFT/ATPG – Will SoC Pressure Make this a Reality?
Organizer: A. Sinha - AMD
Moderator: S. Natarajan - Intel
Panelists: T. M. Mak - Intel Corporation
D. Hamilton - Ateeda Limited
N. Nandra - Synopsys Inc.
S. Sunter - Mentor Graphics
Y. Zorian - Virage Logic

Social Event (14:30 – 22:00)

Wednesday, 4/21/10

Sessions 9 (8:30 – 9:30)

Special Session 9A: Invited Hot Topic: Recent Advanced in Testing 3D-SICs
Organizer: E. Marinissen - IMEC
Moderator: B. Courtois - CMP
On-Chip Testing of Blind and Open-Sleeve TSVs for 3D IC before Bonding
P. Chen, C. Wu - National Tsing Hua University, D. Kwai - Industrial Technology Research Institute
A Structured and Scalable Test Access Architecture for TSV-Based 3D Stacked ICs
E. Marinissen - IMEC, J. Verbree - Delft University of Technology, M. Konijnenburg - Holst Centre/IMEC
Test Resource Partitioning for Memories in a 3D Context
Y. Zorian - Virage Logic

Special Session 9B: New Topic
Organizer: B. Kaminska - Simon Fraser University
Moderator: André Ivanov - UBC
Test Facilities and Infrastructure in Canada
I. McWalter - CMC Microsystems

IP Session 9C: Implications of Power Delivery Network for Validation and Testing
Organizer: S. Natarajan - Intel
Moderator: A. Sinha - AMD
Power Delivery Dynamics and its Impact on Silicon Validation
E. Chiprout -Intel
Tackling IR drop and di/dt Noise during Test
A. Majumdar - AMD
Power Noise and its Impact on Production Test and Validation of SoC Devices
K. Arabi, Qualcomm

Break (9:30 – 9:45)

Sessions 10 (9:45 – 10:45)

Session 10A: Analog/Mixed-Signal Test

Moderator: S. Bernard - LIRMM

An ADC/DAC Loopback Testing Methodology by DAC Output Offsetting and Scaling

X. Huang, J. Huang - National Taiwan University

Calibration-Assisted Production Testing for Digitally-Calibrated ADCs

H. Chang - UC Santa Barbara, K. Lin - Industrial Technology Research Institutie, K. Cheng - UC Santa Barbara

Ordering of Analog Specification Tests Based on Parametric Defect Level Estimation

N. Akkouche, S. Mir, E. Simeu - TIMA Laboratory

Session 10B: Optimization

Moderator: Y. Sato - Kyushu Institute of Technology

A Novel Hybrid Delay Testing Scheme with Low Test Power, Volume, and Time

Z. Chen - Tsinghua University, S. Seth - University of Nebraska, D. Xiang - Tsinghua University

VDDmin Test Optimization for Overscreening Minimization through Adaptive Scan Chain Masking

M. Chen, A. Orailoglu - University Of California At San Diego

Too Many Faults, Too Little Time: On Creating Test Sets for Enhanced Detection of Highly Critical Faults and Defects

Y. Shi, W. Hu, J. Dworak - Brown University

IP Session 10C: 3D Chip Testing

Organizer: Y. Zorian - Virage Logic

Moderator: M. Tahoori - KIT

3D Self Testing with Spidergon STNoC

M. Coppola - STMicroelectronics

Test for 3D: Truth and Fiction

M. Laisne - Qualcomm

Presentation 3- TBA

Presenter 3 - Affiliation

Sessions 11 (11:00 – 12:00)

Session 11A: RF Test

Moderator: M. Margala - University of Massachusetts, Lowell

A Holistic Approach to Accurate Tuning of RF Systems for Large and Small Multi-parameter Perturbations

V. Natarajan, S. Sen, S. Devarakond, A. Chatterjee - Georgia Institute of Technology

Concurrent Process and Specification Cause-Effect Monitoring Using Alternate Diagnostic Signatures (ADS)

S. Devarakond, S. Sen, - Georgia Institute of Technology, S. Bhattacharya - Texas Instruments, A. Chatterjee - Georgia Institute of Technology

Multitone Digital Signal Based Test for Broadband RF Receivers

M. Zeidan, G. Banerjee - Qualcomm Incorporated, R. Gharpurey, J. Abraham - University of Texas

Special Session 11B: Hot Topic: Hardware Security: Design, Test and Verification Issues

Organizers: *S. Bhunia - Case Western Reserve University*
A. Ragunathan - Purdue University

Moderator: *S. Bhunia - Case Western Reserve University*

Presenters: *P. Rohatgi - Cryptography Research*
Side-channel Analysis: Attacks and Countermeasures
S. Weingart - ATSEC
System-level Test and Validation for Tamper-resistance
Y. Makris - Yale University
Hardware Trojans and Trust in ICs

Special Session 11C: Hot Topic: Design Consideration and Silicon Evaluation of On-Chip Monitors

Organizer: S.Chakravarty - LSI
Moderator: M. Spica - Cypress
Presenters: S. Mukhopadhay - Georgia Tech
Variability Characterization for Narrow-Width Devices and Application to Post-Silicon Repair in SRAM
C. Kim - University of Minnesota
Silicon Odometers: On-Chip Test Structures for Accurately Monitoring Circuit Degradation Due to HCI, BTI, and TDDB
S. Chakravarty - LSI Corporation
A Correlation Study of Process Monitors and Manufacturing Tests

Sessions 12 (13:15 – 14:45)

Special Session 12A: Panel: Adaptive Analog Test: Feasibility and Opportunities Ahead

Organizer: H. Stratigopoulos - TIMA Lab
Moderator: R. Daasch- Portland State University
Panelists: S. Benner - Qualcomm
A. Chatterjee - Georgia Tech
R. Looijen - Salland Engineering
Y. Makris - Yale University
P. Nigh - IBM
G. Srinivasan - Texas Instruments

Special Session 12B: Embedded Tutorial: Test and Fault Tolerance of Networks-on-Chip

Organizers: E. Cota, M. Lubaszewski - UFRGS
Moderator: J. Dworak - Brown University
Presenter: M. Lubaszewski - UFRGS

Special Session 12C: Apprentice - VTS Edition: Season 3 – Judging Session

Organizer/Moderator: K. S. Kim - Samsung