Technical Program

28th IEEE

VLSI TEST SYMPOSIUM

(VTS 2010)

Santa Cruz, CA, USA
19-22 April 2010

ttte™

IEEE

IEEE COMPUTER SOCIETY

28th IEEE VLSI Test Symposium (VTS 2010)
Santa Cruz, CA, April 19-22, 2010

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H. Wunderlich - *Universitat Stuttgart*

28th IEEE VLSI Test Symposium (VTS 2010)
Santa Cruz, CA, April 19-22, 2010

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28th IEEE VLSI Test Symposium (VTS 2010)
Santa Cruz, CA, April 19-22, 2010
Santa Cruz, CA, USA
Welcome Message

Welcome to VTS 2010, the twenty-eighth in a series of annual symposia that focus on innovation in the field of testing of integrated circuits and systems.

The core of VTS 2010, the three day technical program, responds to the many trends and challenges in the semiconductor design and manufacturing industries with papers covering a diverse and seminal set of topics including, ATPG and compression, test optimization, power issues in test, delay and performance test, mixed-signal and RF testing, emerging technologies test, yield modelling and defects, memory test & repair, and reliability issues such as transients and soft errors, NBTI, and gate-oxide early life failure.

In addition to the three-day technical program, VTS 2010 features several special sessions including several panels addressing various hot topics, several new topic speakers, and two student activity sessions. VTS 2010 continues the tradition of featuring the Innovative Practices track. The sessions that make up this track highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. This year the Workshop on Test of Wireless Circuits and Systems will take place in conjunction with VTS for the third year.

Two tutorials are offered by the TTTC Tutorials & Education Group through the Test Technology Education Program (TTEP). This year the tutorials cover the exciting topics of “Analog/Mixed-signal/RF Testing” and “On-chip Calibration/Repair Solutions associated with Parameter Variations and Low-Power Design”. Tutorials provide opportunities for design and test professionals to update their knowledge, and earn official IEEE TTTC accreditation.

The social program at VTS provides an opportunity for informal technical discussions among participants. Santa Cruz, with its beaches and mountains, provides a very attractive backdrop for all VTS 2010 activities.

28th IEEE VLSI Test Symposium (VTS 2010)
Santa Cruz, CA, April 19-22, 2010
Santa Cruz, CA, USA
Welcome Message

VTS, like any complex organization, is the sum of the efforts of a large number of volunteers, who selflessly have volunteered their time with their only reward essentially being the satisfaction of seeing a job well done, basking in the realization that they have contributed to the dissemination of scientific knowledge through the continued success of a forum dedicated to the exchange of advances in both research and practice in VLSI Test. No words would compare to the magnitude of the efforts displayed by the volunteers, however we would nonetheless like to register herein a small note of thanks to the whole body of volunteers on whose efforts we have come to deeply rely. We deeply appreciate the financial assistance provided by VTS corporate supporters. For VTS 2010 we are fortunate to have Verigy as an Elite Level Corporate Supporter. We are also fortunate to have Advantest, Intel, Mentor Graphics, Optimal Test, Teradyne and Synopsys as Premier level Corporate Supporters. We also acknowledge the generosity of Freescale Semiconductor for hosting the VTS Program Committee paper selection meeting.

We hope that you will find VTS 2010 enlightening, thought-provoking, rewarding, and enjoyable. I wish you all a fun-filled and productive week in the Santa Cruz area and hope that you will keep making VTS a success by actively participating in it, assisting in its organization, and letting us always know when we can do something better. Thank you all for coming.

General Chair
Magdy Abadir

Program Co-Chairs
Michel Renovell
Claude Thibeault

28th IEEE VLSI Test Symposium (VTS 2010) Official Sponsors

The VLSI Test Symposium is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society

The IEEE promotes the engineering process of creating, developing, integrating, sharing, and applying knowledge about electronic and information technologies and sciences for the benefit of humanity and the profession

The purposes of this IEEE Society shall be scientific, literary, and educational in character. The Society shall strive to advance the theory, practice, and application of computer and information processing science and technology and shall maintain a high professional standing among its members. The scope of the Society shall encompass all aspects of theory, design, practice, and application relating to computer and information processing science and technology

TTTC's goals are to contribute to our members' professional development and advancement, to help them solve engineering problems in electronic test, and to help advance the state-of-the art. In particular, TTTC aims at facilitating the knowledge flow in an integrated manner, to ensure overall quality in terms of technical excellence, fairness, openness, and equal opportunities

28th IEEE VLSI Test Symposium (VTS 2010)
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28th IEEE VLSI Test Symposium (VTS 2010)
GENERAL INFORMATION
REGISTRATION

The IEEE VLSI Test Symposium explores emerging trends and novel concepts in the testing of integrated circuits and systems. The symposium is a leading international forum where many of the world's leading test experts and professionals from both industry and academia join to present and debate key issues in testing. VTS 2010 addresses key trends and challenges in the semiconductor design and manufacturing industries through an exciting program that includes Keynote and Plenary Talks, Technical Paper Sessions, Embedded Tutorials, Panels, Hot Topic Sessions, Full-day Tutorials, co-located Workshop, and the Innovative Practices Track.

Symposium Registration

VTS 2010 April 19th – 22nd	**Advance Rate** (Until April 2nd, 2010)	**On-site Rate** (After April 2nd, 2010)
IEEE/CS Member Registration (Member rates are available only to current members of IEEE/CS. Please enter your valid membership number in order to qualify!)	**$525.00**	**$630.00**
Non-Member Registration	**$660.00**	**$800.00**
Student, Lifetime/Retired Registration (Valid student ID may be required at onsite registration check-in.)	**$225.00**	**$275.00**
Student Non-Member Registration	**$325.00**	**$375.00**
Additional Social Ticket (One Social Ticket is included for those paying IEEE/CS Member or Non-Member VTS rates. Students and companions of registered attendees must purchase a ticket to participate in the social event)	**$100.00**	**$100.00**

28th IEEE VLSI Test Symposium (VTS 2010)
GENERAL INFORMATION
REGISTRATION

Workshop Registration

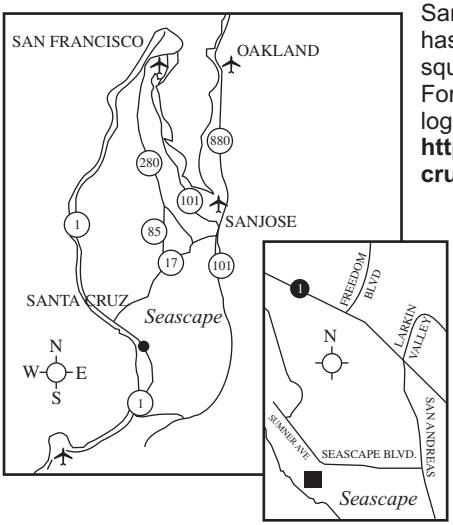
WTW 2010 Full Workshop April 21 - 22nd	**Advance Rate** (Until April 2nd, 2010)	**On-site Rate** (After April 2nd, 2010)
IEEE/CS Member Registration (Member rates are available only to current members of IEEE/CS. Please enter your valid membership number in order to qualify!)	**$220.00**	**$275.00**
Non-Member Registration	**$275.00**	**$345.00**
Student, Lifetime/Retired Registration (Valid student ID may be required at onsite registration check-in.)	**$115.00**	**$175.00**
One Day Member Registration	**$150.00**	**$225.00**
One Day Non-Member Registration	**$190.00**	**$290.00**

TTEP Tutorials Registration

Tutorial No. 1 – April 22nd Practices in Analog, Mixed-signal and RF Testing **Tutorial No. 2 – April 22nd** Parameter Variations and Low-Power Design: Test Issues and On-chip Calibration/Repair Solutions	**Advance Rate** (Until April 2nd, 2010)	**On-site Rate** (After April 2nd, 2010)
IEEE/CS Member Registration (Member rates are available only to current members of IEEE/CS. Please enter your valid membership number in order to qualify!)	**$320.00**	**$385.00**
Non-Member Registration	**$400.00**	**$480.00**

Location:

The City of Santa Cruz, California, is situated on the northern part of Monterey Bay about 74 miles south of San Francisco and 30 miles from San Jose. Santa Cruz is the county seat for the County of Santa Cruz.The City has of an area of 12 square miles.
For more information log on to :
http://www.ci.santa-cruz.ca.us/



About Seascape Beach Resort

Located just south of Santa Cruz, Seascape Beach Resort offers 285 luxurious suites and villas overlooking the Monterey Bay. You'll find all the comforts of home, plus the services and amenities of a four-diamond resort. Do anything you like or do nothing at all. With 17 miles of private beach, fine dining, and a full range of activities to choose from, Seascape Beach Resort has everything you need to make your experience memorable.

The resort is 30 miles away from San Jose Airport.

To contact the hotel:
Seascape Resort
One Seascape Resort Dr.
Aptos, CA 95003
831-662-7126 (Phone)
831-685-3059 (FAX)

The reservation cut-off date is 27 March 2010 at 5:00 p.m. Pacific time. Reservations received after this date will be accepted by the Hotel on a space available basis at the conference rates. Modifications made to existing reservations after this date will be treated as advance reservations.

Group rate

Deluxe Suite	$163.90
One Bedroom Beach Villa	$207.90
Two Bedroom Beach Villa	$328.90

The Group Rate covers all guest sleeping room costs including standard resort fees and the 10% sales/room tax. Rate is inclusive of bell and housekeeping gratuities. The rate also includes in-suite high-speed Internet access, on-property transportation and access to the full-service Seascape Sports Club.

28th IEEE VLSI Test Symposium (VTS 2010)
TECHNICAL PROGRAM AGENDA
Monday, April 19th, 2010

07:30AM - 09:00AM BREAKFAST

09:00AM - 11:00AM
Seascape Grand Ballroom

PLENARY SESSION

Welcome Message:
Magdy Abadir, General Chair

Program Introduction:
Michel Renovell and Claude Thibeault,
Program Co-Chairs

Keynote Speaker:
Robert Madge, Director of Technology, LSI Logic

Invited Keynote:
Ron Collett, CEO & President, Nemetrics

Awards presentation:
IEEE Fellow Awards
TTTC Most Successful Technical Meeting Award
TTTC Most Populous Technical Meeting Award
VTS 2009 Best Paper Award
VTS 2009 Best Panel Award
VTS 2009 Best Innovative Practices Award

11:00AM - 11:15AM BREAK

11:15AM - 12:15PM
Del Mar

Session 1A: **DELAY & PERFORMANCE TEST 1**
Moderator: M. Batek - Broadcom

1A.1 *Fast Path Selection for Testing of Small Delay Defects Considering Path Correlations*
Z. He, T. Lv - Institute of Computing Technology,
H. Li, X. Li - Chinese Academy of Sciences

1A.2 *Identification of Critical Primitive Path Delay Faults without any Path Enumeration*
K. Christou, M. Michael, S. Neophytou - U. of Cyprus

1A.3 *Path Clustering for Adaptive Test*
T. Uezono, T. Takahashi - Tokyo Institute of Technology,
M. Shintani , K. Hatayama - Semiconductor Technology Academic Research Center, K. Masu - Tokyo Institute of Technology, H. Ochi, T. Sato - Kyoto U.

11:15AM - 12:15PM
Seascape 3

Session 1B: **MEMORY TEST & REPAIR**
Moderator: P. Prinetto - Politecnico di Torino

1B.1 *Automatic Generation of Memory Built-In Self-Repair Circuits in SOCs for Minimizing Test Time and Area Cost*
T. Tseng, C. Hou, J. Li - National Central U

1B.2 *Bit Line Coupling Memory Tests for Single Cell Fails in SRAMs*
S. Irobi, Z. Al-ars, S. Hamdioui - Delft U of Technology

1B.3 *Reducing Test Time and Area Overhead of an Embedded Memory Array Built-In Repair Analyzer with Optimal Repair Rate*
J. Chung, J. Park - The U of Texas at Austin,
E. Byun, C. Woo - Samsung Electronics,
J. Abraham - The U of Texas at Austin

11:15AM - 12:15PM
Riviera

IP Session 1C: **INNOVATIVE PRACTICES IN RF TEST**
Organizer: R. Parekhji - Texas Instruments
Moderator: TBA

1C.1 *Test Time Reduction Using Parallel RF Test Techniques*
R. Mittal, A. Sontakke, R. Parekhji,
Texas Instruments, Bangalore

1C.2 *Density Estimation for Analog/RF Test Problem Solving*
S. Mir, H. Stratigopoulos -TIMA, A. Bounceur - European U of Brittany

1C.3 *Low Cost Test and Tuning of RF Circuits and Systems*
F. Taenzler - Texas Instruments, A. Chatterjee - Georgia Institute of Technology

12:15PM - 01:30PM LUNCH

Innovative Practice Sessions

28th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Monday, April 19th, 2010

01:30PM - 02:30PM
Del Mar

Session 2A: **Delay & Performance Test 2**
Moderator: F. Ferhani - Broadcom

2A.1 *A Novel Hybrid Method for SDD Pattern Grading and Selection*
K. Peng, J. Thibodeau - U of Connecticut,
M. Yilmaz - AMD, K. Chakrabarty - Duke U,
M. Tehranipoor - U of Connecticut

2A.2 *Forming Multi-Cycle Tests for Delay Faults by Concatenating Broadside Tests*
I. Pomeranz - Purdue U, S. Reddy - U of Iowa

2A.3 *An Output Compression Scheme for Handling X-states from Over-Clocked Delay Tests*
A. Singh, C. Han, X. Quian - Auburn U

01:30PM - 02:30PM
Seascape 3

Session 2B: **Dealing with NBTI and Gate-Oxide Early Life Failure**
Moderator: L. Winemberg - Freescale

2B.1 *Reliable Cache Design with On-Chip Monitoring of NBTI Degradation in SRAM Cells using BIST*
F. Ahmed, L. Milor - Georgia Institute of Technology

2B.2 *Gate-Oxide Early Life Failure Identification using Delay Shifts*
Y. Kim, T. Chen - Stanford U, Y. Kameda,M. Mizuno - NEC Corporation, S. Mitra - Stanford U

2B.3 *Detecting NBTI Induced Failures in SRAM Core-Cells*
R. Alves Fonseca, L. Dilillo, A. Bosio, P. Girard,
S. Pravossoudovitch, A. Virazel - LIRMM,
N. Badereddine - Infineon

01:30PM - 02:30PM
Riviera

IP Session 2C: **Design, Fabrication, and Test of Flexible Electronics**
Organizer K. Cheng - UC Santa Barbara
Moderator: B. Kaminska – Simon Fraser U.

2C.1 *Design, Analysis, and Test of Low-Power and Reliable Flexible Electronics*
K. Cheng, T. Huang - UC Santa Barbara

2C.2 *Fabrication and Testing of Large-area Flexible Electronics for Displays and Sensor Arrays*
W. Wong - Palo Alto Research Center

2C.3 *Overview of Flexible Electronics from ITRI's Viewpoint*
J. Hu - ITRI

Innovative Practice Sessions

02:30PM - 02:45PM BREAK

02:45PM - 03:45PM
Del Mar

Session 3A: **Delay & Performance Test 3**
Moderator: B. Becker - U of Freiburg

3A.1 *Impact of Multiple Input Switching on Delay Test under Process Variation*
S. Wu – UC Santa Barbara, S. Chakravarty - LSI, L. Wang - UC Santa Barbara

3A.2 *Low-Power Test Planning for Arbitrary At-Speed Delay-Test Clock Schemes*
C. Zoellin, H. Wunderlich - Universität Stuttgart

3A.3 *Selecting the Most Relevant Structural Fmax for System Fmax Correlation*
J. Chen – UC Santa Barbara, J. Zeng - Advanced Micro Devices, L. Wang - UC Santa Barbara

02:45PM - 03:45PM
Seascape 3

Session 3B: **Emerging Technologies Test**
Moderator: R. Aitken - ARM

3B.1 *On-the-fly Variation Tolerant Mapping in Crossbar Nano-Architectures*
M. Tahoori, C. Tunc - Northeastern U

3B.2 *Pin-Count-Aware Online Testing of Digital Microfluidic Biochips*
Y. Zhao, K. Chakrabarty - Duke U

3B.3 *iMajik: Making 1149.1 TAPs Disappear and Reappear in SoCs and 3D Packages*
C. Clark - Intellitech Corporation

02:45PM - 03:45PM
Rivera

IP Session 3C: **INDUSTRIAL PRACTICES OF TEST COST REDUCTION TECHNIQUES: IMPACT AND DESIGN TRADEOFFS**
Organizer: S. Tammali - Texas Instruments Inc.
Moderator: Phil Nigh, IBM

3C.1 *Industrial Practices of Test Cost Reduction: Perspective, Current design practices*
S. Tammali - Texas Instruments Inc.

Innovative Practice Sessions

3C.2 *Adaptive Test Delivers Wide Range of Sophisticate Test Solutions*
K. Arnold - Pintail Technologies

3C.3 *Test Cost and Test Power Conflicts: EDA Perspective*
M. Hirech - Synopsys

03:45PM - 04:00PM BREAK

04:00PM - 05:30PM
Del Mar

Special Session 4A: **Apprentice - VTS Edition: Season 3**
Organizer/Moderator: K. S. Kim - Samsung

04:00PM - 05:30PM
Seascape 3

Special Session 4B: **LOW-POWER TEST AND NOISE-AWARE TEST: FOES OR FRIENDS?**
Organizer: : I. Polian - *U of Freiburg*
Moderator: S. Reddy - *U of Iowa*
Panelists:
W. Cheng - Mentor Graphics
C. Tirumurti - Intel
X. Wen - KIT
Y. Zorian - Virage Logic

04:00PM - 05:30PM
Riviera

Special Session 4C: **Thesis Research Posters**
Organizers: H. Stratigopoulos - TIMA Lab
Moderator: P. Bernardi - Politecnico di Torino

Innovative Practice Sessions

28th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Tuesday April 20th, 2010

07:00AM - 08:00AM BREAKFAST

08:00AM - 09:00AM
Del Mar

Session 5A: **LOW-POWER IC TEST**
Moderator: M. Tehranipoor - U of Connecticut

5A.1 *A Generic Low Power Scan Chain Wrapper for Designs Using Scan Compression*
A. Sabne – Bhel, R. Tiwari, A. Shrivastava, S. Ravi, R. Parekhji - Texas Instruments

5A.2 *Low-Capture-Power At-Speed Testing using Partial Launch-on-Capture Test Scheme*
Z. Chen, D. Xiang - Tsinghua U

5A.3 *Theoretical Analysis for Low-Power Test Decompression Using Test-Slice Duplication*
S. Mu, M. Chao - National Chiao-tung U

08:00AM - 09:00AM
Seascape 3

Session 5B: **TRANSIENTS & SOFT ERRORS**
Moderator: M. Zang - Intel

5B.1 *CSER: BISER-Based Concurrent Soft-Error Resilience*
L. Wang - Syntest Technologies, Inc., N. Touba - U of Texas at Austin, Z. Jiang, S. Wu - Syntest Technologies, Inc., J. Huang, J. Li - National Taiwan U

5B.2 *Workload-Driven Selective Hardening of Control State Elements in Modern Microprocessors*
M. Maniatakos, Y. Makris - Yale U

5B.3 *Scalable and Accurate Estimation of Probabilistic Behavior in Sequential Circuits*
C. Yu, J. Hayes - U of Michigan

08:00AM - 09:00AM
Riviera

IP Session 5C: **Post-Silicon Debug**
Organizer: S. Gupta - USC
Moderator: TBA
Post-silicon debug leveraging embedded memory based solutions
G. Torjyan, Y. Zorian - Virage Logic
Presenter 1 - Presenters to Include:
K. Tiruvallur - Intel Corp
Presenter 2 - Presenters to Include:
Presenter 3 - Presenters to Include:

Innovative Practice Sessions

28th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Tuesday April 20th, 2010

09:00AM - 09:15AM BREAK

09:15AM - 10:15AM

Del Mar

Session 6A: **POWER ISSUES IN TEST**
Moderator: H. Wunderlich - U of Stuttgart

6A.1 *At-Speed Scan Test with Low Switching Activity*
L. Xie, A. Davoodi, K. Saluja, A. Sinkar - U of
E. Moghaddam - U of Iowa , J. Rajski - Mentor Graphics, S. Reddy - U of Iowa,
M. Kassab - Mentor Graphics

6A.2 *Low-Power Compression Architecture*
S. Bhatia - Atrenta

6A.3 *Thermal-Uniformity-Aware X-Filling to Reduce Temperature-Induced Delay Variation for Accurate At-Speed Testing*
T. Yoneda, M. Inoue - Nara Institute of Science and Technology, Y. Sato - Kyusyu Institute of Technology,
H. Fujiwara - Nara Institute of Science and Technology

09:15AM - 10:15AM

Seascape 3

Session 6B**: YIELD MODELING & DEFECTS**
Moderator: H. Manhaeve - Q-StarTest

6B.1 *Modeling Yield, Cost, and Quality of an NoC with Uniformly and Non-Uniformly Distributed Redundancy*
S. Shamshiri, K. Cheng - UC Santa Barbara

6B.2 *Evaluating Yield and Testing Impact of Sub-Wavelength Lithography*
W. Tam , R. Blanton , W. Maly - Carnegie Mellon U

6B.3 *Defect Diagnosis Based on DFM Guidelines*
D. Kim,, I. Pomeranz - Purdue U,
M. Amyeen , S. Venkataraman - Intel Corporation

09:15AM - 10:15AM

Riviera

IP Session 6C: **NEW TOPIC**
Organizer: B. Kaminska - Simon Fraser U
Moderator: TBA

6C.1 *Mixed-Signal Test Impact to SoC Commercialization*
K.Arabi - Qualcomm

Innovative Practice Sessions

28th IEEE VLSI TEST SYMPOSIUM
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Tuesday April 20th, 2010

10:15AM - 10:30AM BREAK

10:30AM-11:30AM

Del Mar

Session 7A: **ATPG & COMPRESSION**
Moderator: S. Hellebrand – U of Paderborn

7A.1 *Application of Signal and Noise Theory to Digital VLSI Testing*
N. Yogi , V. Agrawal - Auburn U

7A.2 *On Multiple Bridging Faults*
I. Pomeranz - Purdue U, S. Reddy - U Of Iowa

7A.3 *Reusing NoC-Infrastructure for Test Data Compression*
V. Froese , R. Ibers, S. Hellebrand - U Of Paderborn

10:30AM-11:30PM

Seascape 3

Session 7B: **ON-LINE & SYSTEM TESTING**
Moderator: A. Orailoglu - UC San Diego

7B.1 *Concurrent Autonomous Self-Test for Uncore Components in System-on-Chips*
Y. Li - Stanford U, O. Mutlu - Carnegie Mellon U, D. Gardner - Intel Labs,S. Mitra - Stanford U

7B.2 *Low-sensitivity to Process Variations Aging Sensor for Automotive Safety-Critical Applications*
J. Vazquez, V. Champac - Istituto Nacional de Astrofisica, A. Ziesemer Jr., R. Reis -UFRGS, I. Teixeira, M. Santos, J. Teixeira - Lisboa Technical U.

7B.3 *Board-level Fault Diagnosis using Bayesian Inference*
Z. Zhang, Z. Wang - Duke U, X. Gu - Cisco Systems, Inc., K. Chakrabarty - Duke U

10:30AM-11:30PM

Riviera

IP Session 7C: **VERIFICATION AND TESTING CHALLENGES IN HIGH-LEVEL SYNTHESIS**

Organizers: S. Ray - U of Texas at Austin, J. Bhadra - Freescale Semiconductor
Moderator: S. Ray - U. of Texas at Austin

7C.1 *The Roadblocks to Broad Adoption of High Level Synthesis*
M. Keating - Synopsys Inc.

Innovative Practice Sessions

7C.2 *High Level Synthesis of a Front End Filter and DSP Engine for Analog to Digital Conversion - A Case Study*
S. Ramirez-Chavez - Cadence Design Systems Inc.

7C.3 *Easing the Verification Bottleneck using High-level Synthesis*
D. Varma, D. Mackay, P. Thiruchelvam - AutoESL Design Technologies

11:30PM - 12:45PM LUNCH

12:45PM - 02:15PM

Riviera

Special Session 8A: **E.J. MCCLUSKEY DOCTORAL THESIS COMPETITION**
Organizer: H. Stratigopoulos - TIMA Lab
Moderator: P. Bernardi - Politecnico di Torino

12:45PM - 02:15PM

Seascape 3

Special Session 8B: **New Topic**

Organizers: B. Courtois - CMP
Moderator: L. Anghel – TIMA Lab.
MOS/MTJ-Hybrid Circuit with Nonvolatile Logic-in-Memory Architecture and Its Impact
T. Hanyu - Tohoku U.

12:45PM - 02:15PM

Del Mar

Special Session 8C: **Panel: EDA for Analog DFT/ATPG – Will SoC Pressure Make this a Reality?**
Organizer: A. Sinha - AMD
Moderator: S. Natarajan - Intel
Panelists: S. Abdennadher - Intel Corporation
D. Hamilton - Ateeda Limited
N. Nandra - Synopsys Inc.
S. Sunter - Mentor Graphics
Y. Zorian - Virage Logic

02:15PM - 10:00PM

SOCIAL PROGRAM

28th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Wednesday April 21st, 2010

07:30AM - 08:30AM BREAKFAST

08:30AM - 09:30AM

Del Mar

Special Session 9A: **INVITED HOT TOPIC: RECENT ADVANCES IN TESTING 3D-SICS**
Organizer: E. Marinissen - IMEC
Moderator: B. Courtois - CMP

9A.1 *On-Chip Testing of Blind and Open-Sleeve TSVs for 3D IC before Bonding*
P. Chen, C. Wu - National Tsing Hua U,
D. Kwai - Industrial Technology Research Institute

9A.2 *A Structured and Scalable Test Access Architecture for TSV-Based 3D Stacked ICs*
E. Marinissen - IMEC, J. Verbree - Delft U of Technology, M. Konijnenburg - IMEC

9A.3 *Test Resource Partitioning for Memories in a 3D Context*
Y. Zorian - Virage Logic

08:30AM - 09:30AM

Seascape 3

Special Session 9B: **NEW TOPIC**
Organizer: B. Kaminska - Simon Fraser U
Moderator: TBA

Test Facilities and Infrastructure in Canada
I. McWalter - CMC Microsystems

08:30AM - 09:30AM

Riviera

IP Session 9C: **Implications of Power Delivery Network for Validation and Testing**

Organizers: S. Natarajan - Intel
Moderator: A. Sinha - AMD

9C.1 *Power Delivery Dynamics and its Impact on Silicon Validation*
E. Chiprout -Intel

9C.2 *Tackling IR drop and di/dt Noise during Test*
A. Majumdar - AMD

9C.3 *Power Noise and its Impact on Production Test and Validation of SoC Devices*
K. Arabi, Qualcomm

09:30AM - 09:45AM BREAK

28th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Wednesday April 21st, 2010

09:45AM - 10:45AM

Del Mar

Special Session 10A: **ANALOG/MIXED-SIGNAL TEST**
Moderator: S. Bernard - LIRMM
Presenter: A. Sacco - Northeastern U.

10A.1 *An ADC/DAC Loopback Testing Methodology by DAC Output Offsetting and Scaling*
X. Huang, J. Huang - National Taiwan U.

10A.2 *Calibration-Assisted Production Testing for Digitally-Calibrated ADCs*
H. Chang - UC Santa Barbara, K. Lin - Industrial Technology Research Institutie,
K. Cheng - UC Santa Barbara

10A.3 *Ordering of Analog Specification Tests Based on Parametric Defect Level Estimation*
N. Akkouche, S. Mir, E. Simeu - TIMA Laboratory

09:45AM - 10:45AM

Seascape 3

Session 10B: **OPTIMIZATION**
Moderator: Y. Sato - Kyushu Institute of Technology

10B.1 *A Novel Hybrid Delay Testing Scheme with Low Test Power, Volume, and Time*
Z. Chen - Tsinghua U, S. Seth - U of Nebraska,
D. Xiang - Tsinghua U

10B.2 *VDDmin Test Optimization for Overscreening Minimization through Adaptive Scan Chain Masking*
M. Chen, A. Orailoglu - U Of California At San Diego

10B.3 *Too Many Faults, Too Little Time: On Creating Test Sets for Enhanced Detection of Highly Critical Faults and Defects*
Y. Shi, W. Hu, J. Dworak - Brown U

09:45AM - 10:45AM

Riviera

IP Session 10C: **3D Chip Testing**
Organizers: Y. Zorian - Virage Logic
Moderators: M. Tahoori - KIT

10C.1 *Test for 3D: Truth and Fiction*
Michael Laisne - Qualcomm

10C.2 *3D Self Testing with Spidergon STNoC*
M. Coppola - STMicroelectronics

Innovative Practice Sessions

10:45AM - 11:00AM BREAK

11:00PM - 12:00PM
Del Mar

Session 11A: **RF TEST**
Moderator: M. Margala - U of Massachusetts, Lowell

11A.1 *A Holistic Approach to Accurate Tuning of RF Systems for Large and Small Multi-parameter Perturbations*
V. Natarajan, S. Sen, S. Devarakond, A. Chatterjee - Georgia Institute of Technology

11A.2 *Concurrent Process and Specification Cause-Effect Monitoring Using Alternate Diagnostic Signatures (ADS)*
S. Devarakond, S. Sen, - Georgia Institute of Technology, S. Bhattacharya - Texas Instruments, A. Chatterjee - Georgia Institute of Technology

11A.3 *Multitone Digital Signal Based Test for Broadband RF Receivers*
M. Zeidan, G. Banerjee - Qualcomm Incorporated, R. Gharpurey, J. Abraham - U of Texas

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11:00PM - 12:00PM
Seascape 3

Session 11B: **HOT TOPIC: HARDWARE SECURITY: DESIGN, TEST AND VERIFICATION ISSUES**
Organizers: S. Bhunia - Case Western Reserve U
A. Ragunathan - Purdue U
Moderator: S. Bhunia - Case Western Reserve U
Presenters: P. Rohatgi - Cryptography Research
Side-channel Analysis: Attacks and Countermeasures
S. Weingart - ATSEC
System-level Test and Validation for Tamper-resistance
Y. Makris - Yale U
Hardware Trojans and Trust in ICs

11:00PM - 12:00PM
Riviera

Session 11C: **HOT TOPIC: DESIGN CONSIDERATION AND SILICON EVALUATION OF ON-CHIP MONITORS**
Organizers: S.Chakravarty - LSI
Moderator: M. Spica - Cypress
Presenters: S. Mukhopadhay - Georgia Tech

11C.1 *Variability Characterization for Narrow-Width Devices and Application to Post-Silicon Repair in SRAM*
C. Kim - U. of Minnesota

11C.2 *Silicon Odometers: 3D-Chip Test Structures for Accurately Monitoring Circuit Degradation Due to HCI, BTI, and TDDB*
C. Kim - U. of Minnesota

11C.3 *A Correlation Study of Process Monitors and Manufacturing Tests*
S. Chakravarty - LSI Corporation

12:00PM - 01:15PM LUNCH

01:15PM - 02:45PM
Del Mar

Special Session 12A: **PANEL: ADAPTIVE ANALOG TEST: FEASIBILITY AND OPPORTUNITIES AHEAD**
Organizer: H. Stratigopoulos - TIMA Lab
Moderator: R. Daasch- Portland State U
Panelists:
S. Benner - Qualcomm
A. Chatterjee - Georgia Tech
R. Looijen - Salland Engineering
Y. Makris - Yale University
P. Nigh - IBM
G. Srinivasan - Texas Instruments

01:15PM - 02:45PM
Seascape 3

Special Session 12B: **EMBEDDED TUTORIAL: TEST AND FAULT TOLERANCE OF NETWORKS-ON-CHIP**
Organizer/Presenters: E. Cota, M. Lubaszewski - UFRGS
Moderator: TBA

01:15PM - 02:45PM
Riviera

Special Session 12C: **APPRENTICE - VTS EDITION: SEASON 3 – JUDGING SESSION**
Organizer / Moderator: K. S. Kim - Samsung

28th IEEE VLSI TEST SYMPOSIUM
SOCIAL PROGRAM

For this year's social event, we will start at 2:15 PM by taking a bus ride to one of the famous attractions of Santa Cruz – "The Mystery Spot". The Mystery Spot is a gravitational anomaly located in the redwood forests just outside of Santa Cruz, California. It was discovered in 1939 by a group of surveyors. Some speculate that cones of metal were secretly brought here by aliens and buried in our earth as guidance systems for their spacecraft. Some think that it is in fact the spacecraft itself burried deep within the ground. Other theories include carbon dioxide permeating from the earth, a hole in the ozone layer, a magna vortex, the highest dielectric biocosmic radiation known anywhere in the world, and radiesthesia. Whatever that cause is, it remains a mystery.

Buses will continue to take the attendees to the Mystery Spot starting 2:15 and will bring the passengers back to the resort after the tour. We should all be back at the resort by 5:30 PM.

Once we are back at the resort, we will head to the beach! Dinner will be served on the beautiful beach of the Seascape resort. Dinner festivities will start at 6 PM and lasts until 10PM. You will get to enjoy great food and drinks at the beachside accompanied by beautiful California sunset. A fire will be setup as it gets dark into the night. You can continue to enjoy the sounds of the ocean alongside the fire or take a walk on the beach after dinner. Just remember to dress warm as the sea breeze can be a bit cold. There is no extra cost for this program for VTS attendees who register at member and non-member rates. Students and companions of VTS attendees can register for the Social Program for $100 per person. So, come and join us!

Useful information:
Mystery Spot
465 Mystery Spot Road
Santa Cruz, CA 95065-9658,
United States
Tel - (831) 423-8897

28th IEEE VLSI TEST SYMPOSIUM
TEST TECHNOLOGY
EDUCATIONAL PROGRAM 2010

The Tutorials and Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes in 2010 a comprehensive set of Test Technology Tutorials to be held in conjunction with TTTC sponsored technical meetings and included in the annual and expanding Test Technology Educational Program (TTEP). TTEP intends to serve the test and design professionals offering fundamental education and expert knowledge in state-of-the-art test technology topics.

Participation in TTEP-organized tutorials is credited by TTTC. Each full day tutorial corresponds to four TTEP units. Upon completion of each sixteen TTEP units official accreditation in the form of an "IEEE TTTC Test Technology Certificate" will be presented to the participants. In addition to the tutorials, certified university courses and industrial seminars related to test technology can also be included in TTEP and the participation in these credited similar to TTEP tutorials. For information on TTEP 2010 please visit the TTEP web site http://tab.computer.org/tttc/teg/ttep. The test technology tutorials of the VTS 2010 technical program are part of TTEP 2010.

For further information

Dimitris Gizopoulos
Tutorials and Education Group Chair
University of Piraeus, Greece
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Email: dgizop@unipi.gr
TTEP web site: http://tab.computer.org/tttc/teg/ttep

28th IEEE VLSI TEST SYMPOSIUM
TUTORIAL 1
Thursday, April 22nd 2010

VLSI Test Symposium 2010 includes two excellent TTEP 2010 tutorials on high interest test technology topics. The tutorials qualify for IEEE TTTC certification. The tutorials will be presented on Thursday, April 22nd (8:30am-4:40pm). The tutorials require a separate fee and registration (see General Information).

Del Mar 1

8:30AM - 4:40PM

Tutorial: Practices in Analog, Mixed-signal and RF Testing

PRESENTERS: SALEM ABDENNADHER (Intel), SAGHIR A. SHAIKH (Broadcom)

AUDIENCE: This tutorial is most suitable for design, test and DFT engineers involved in actual implementation of mixed-signal, analog, RF and wireless devices and systems. The architects and engineering managers would also greatly benefit from this tutorial

DESCRIPTION: The objective of this course is to present existing industry ATE solutions and the alternative solutions to ATE testing for mixed-signal and RF SoCs. These techniques greatly rely upon DFT and BIST structures. Tutorial presents the basic concepts in analog and RF measurements (eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, EVM, etc.). Several industrial examples of production testing of mixed-signal and RF devices, such as, SERDES transceivers, PHYs, PMDs, and RF transceivers are also presented. The block-DFT solutions are presented for PLLs, delta-sigma converters, equalizers, filters, mixers, AGC, LNAs, DACs and ADCs. The testing of high speed IO interfaces, such as, PCI-Express, and XAUI, etc, and the new design trends in RF systems such as MIMO and SiP based systems and their testability are also presented in this tutorial.

28th IEEE VLSI TEST SYMPOSIUM
TUTORIAL 2
Thursday, April 22nd 2010

Del Mar 2

8:30AM - 4:40PM

Tutorial: Parameter Variations and Low-Power Design: Test Issues and On-chip Calibration/Repair Solutions

PRESENTERS: RAHUL RAO (IBM Research), SAIBAL MUKHOPADYAY (Georgia Institute of Technology), SWARUP BHUNIA (Case Western Reserve University), PRAVEEN ELAKKUMANAN (IBM)

AUDIENCE: This tutorial is targeted towards test and design engineers, tool developers, researchers and students interested in variability and automated characterization and compensation approaches for reliability and power management and yield improvement

DESCRIPTION: Variations in device and interconnection characteristics resulting from process imperfections, environmental, (e.g. temperature, voltage), temporal (e.g. NBTI, HCI, TDDB) and workload effects degrade the parametric yield and systems robustness. Such variations result in increased test cost and reduced yield due to test challenges due to new failure mechanisms and increased parametric failure rate. Low-power design techniques such as voltage scaling, body biasing and dual-Vth further aggravate these issues. Post-manufacturing approaches for on-chip calibration and self-repair of degraded systems constitute a promising class of solutions to improve the parametric yield through pro-active delay compensation and enhanced power management. To provide a comprehensive coverage on parameter variations and its impact on test, this tutorial will focus on: 1) intrinsic device physics and process limitations that cause variations; 2) design and test issues associated with parameter variations; 3) impact on yield and reliability; 3) test issues for low-power designs under variations; and 4) on-chip calibration and repair schemes for logic, memory and mixed-signal circuits to improve parametric yield and reliability. On-chip monitoring systems for self-calibration and in-field predictive diagnosis will be presented. Design and test approaches that address within-die parameter variations will be discussed with emphasis on power management. Finally, the tutorial will discuss online adaptation techniques for reliability improvement under temperature fluctuations and device degradations.

IEEE Workshop on Test of Wireless Circuits and Systems WTW 2010 April 21st - 22nd , 2010

The Wireless Test Workshop (WTW2010) is devoted to exploring all issues relating to the design and test of wireless circuits and systems. The workshop will be held in conjunction with the VLSI Test Symposium (VTS) 2010, on April 19-20. The program will start on the afternoon of April 21st right after the last session of VTS and will continue all day on April 22nd. Please consult the registration section of this brochure for WTW registration information. The advanced program of WTW is available online on the VTS website.

SCOPE: The Wireless Test Workshop (WTW) includes, among others, the following major topics in RF test: Case Studies, High-Frequency Test, Embedded RF Circuit Test, RF Test Board Related Issues, Yield Learning, Wireless Test Methodology, Standards Conformance Test, Noise Characterization and Validation, Economics of Test, Wireless Product Test Equipment and Metrology.

Advance Program Summary:

Keynote Speaker:	Testing at the Subsystem and System Level, Christian Olgaard, CTO LitePoint Corporation
Invited Speaker:	A Close look at the Ongoing Low-Power, Low Data Rate Wireless Technology Revolution, Sylla Iboun, Texas Instruments
Session #2:	Panel: On-Chip Calibration/Compensation/ Measurement
Session #3:	Open Mic on Parallel/Concurrent RF Testing
Session #4:	Advanced RF Test Techniques

REGISTRATION: All WTW 2010 participants require registration, which includes workshop technical sessions, workshop informal proceedings; break refreshments, lunch and dinner.

SPONSORSHIP: WTW 2010 is sponsored by the IEEE Computer Society TTTC.

INFORMATION: For further details on the technical program, please contact Program Chair, Mustapha Slamani (slamanim@us.ibm.com). Regarding other questions, please contact the General Chair, Rob Aitken (rob.aitken@arm.com).

Please visit our web-site:
http://www.public.asu.edu/~sozev/WTW10/

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28TH IEEE VLSI TEST SYMPOSIUM - PROGRAM AT A GLANCE

Monday, April 19th 2010			
7:30 am - 5:00 pm	REGISTRATION		
7:30 am - 9:00 am	BREAKFAST		
09:00AM - 11:00AM	PLENARY SESSION		
11:15am-12:15pm	Session 1A - Delay & Performance Test 1	Session 1B: Memory Test & Repair	Session 1C: Innovative Pratices in RF Test
12:15pm - 01:30 pm	LUNCH		
1:30 pm - 2:30 pm	Session 2A: Delay & Performance Test 2	Session 2B:Dealing with NBTI and Gate-Oxide Early Life Failure	Session 2C:Design, Fabrication, and Test of Flexible Electronics
2:45pm- 3:45 pm	Session 3A: : Delay & Performance Test 3	Seesion 3B: Emerging Technologies Test	Session 3C: Industrial Practices of Test Cost Reduction Techniques: Impact and Design Tradeoffs
4:00 pm - 5:30 pm	Session 4A: Apprentice - VTS Edition: Season 3	Session 4B: Low-Power Test and Noise-Aware Test: Foes or Friends?	Session 4C: Thesis Research Posters
Tuesday,April 20th 2010			
7:00 am - 8:00 am	BREAKFAST		
8:00 am - 9:00 am	Session 5A:Low-Power IC Test	Session 5B: Transients & Soft Errors	Session 5C: Post-Silicon Debug

9:15 am - 10:15 am	Session 6A: Power Issues in Test	Session 6B: Yield Modeling & Defects	Session 6C: New Topic
10:30 am - 11:30am	Session 7A: ATPG & Compression	Session 7B: On-line & System Testing	Session 7C: Verification and Testing Challenges in High-Level Synthesis
11:30 am - 12:45 pm	LUNCH		
12:45 pm - 2:15 pm	E.J. McCluskey Doctoral Thesis CompetitionNew Topic - At Speed Testing in the Face of Process Variations	Session 8B: New Topic	Session 8C: EDA for Analog DFT/ATPG – Will SoC Pressure Make this a Reality?
2:15pm - 10:00 pm	Social Program		
Wednesday,April 21st 2010			
7:30 am - 8:30 am	BREAKFAST		
8:30 am - 9:30 am	Session 9A: Invited Hot Topic: Recent Advanced in Testing 3D-SICs	Session 9B: New Topic	IP Session 9C: Implications of Power Delivery Network for Validation and Testing
9:45 am - 10:45 am	Session 10A: Analog/Mixed-Signal Test	Session 10B: Optimization	IP Session 10C: 3D Chip Testing
11:00 am - 12:00 pm	Session 11A: RF Test	Session 11B:Hot Topic: Hardware Security: Design, Test and Verification Issues	Special Session 11C: Hot Topic: Design Consideration and Silicon Evaluation of On-Chip Monitors
12:00 pm - 1:15 pm	LUNCH		
1:15pm - 2:45 pm	Session 12A: Adaptive Analog Test: Feasibility and Opportunities Ahead	Session 12B: Embedded Tutorial: Test and Fault Tolerance of Networks-on-Chip	Special Session 12C:Apprentice - VTS Edition: Season 3 – Judging Session

Innovative Practice Sessions *Special Sessions*

Notes

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28th IEEE VLSI TEST SYMPOSIUM 2010
FRINGE MEETINGS

A number of TTTC professional groups interested in test will hold their meetings at VTS 2010. At press time, the following meetings were scheduled. These meetings are for members. If you'd like to attend, please contact the person listed at the e-mail address given.

MONDAY, April 19th		
12:15PM - 01:30PM	**Test Week Workshop Coordination** Yervant Zorian *(zorian@viragelogic.com)*	During Lunch
01:30PM - 02:30PM	**TTTC Tutorials and Education Group** Dimitris Gizopoulos *(dgizop@unipi.gr)* Yiorgos Makris *(yiorgos.makris@yale.edu)*	Peninsula
02:30PM - 03:30PM	**TTTC Executive Committee** Adit Singh *(adsingh@eng.auburn.edu)*	Peninsula
04:30PM - 05:30PM	**TTTC Senior Leadership Board** Yervant Zorian *(zorian@viragelogic.com)*	Peninsula
05:30PM - 07:30PM	**IEEE VTS Program Committee** Michel Renovell *(renovell@lirmm.fr)* Claude Thibeault *(claude.thibeault@etsmtl.ca)*	Seascape 2
07:30PM - 09:30PM	**IEEE VTS and TTTC Recognition Dinner (By Invitation Only)** Michel Renovell *(renovell@lirmm.fr)* Claude Thibeault *(claude.thibeault@etsmtl.ca)*	Seascape 1
TUESDAY, April 20th		
08:00AM - 09:30AM	**TTTC Technical Meetings Review Committee** Chen-Huan Chiang *(chenhuan@alcatel-lucent.com)*	Peninsula
11:30AM - 12:45PM	**TTTC Standards Group** Rohit Kapur *(rohit.kapur@synopsys.com)*	During Lunch
11:30AM - 12:45PM	**Int'l OnLine Test Symposium Committee** Michael Nicolaidis *(michael.nicolaidis@imag.fr)*	During Lunch
01:00PM - 02:00PM	**TTTC Communications Group** Cecilia Metra *(cecilia.metra@unibo.it)*	Peninsula
WEDNESDAY, April 21st		
08:00AM - 09:30AM	**TTTC Operations Committee** Adit Singh *(adsingh@eng.auburn.edu)*	Peninsula
09:30AM - 11:30PM	**IEEE VTS Organizing Committee** Magdy Abadir *(m.abadir@freescale.com)*	Peninsula