



27th IEEE VLSI TEST SYMPOSIUM

Santa Cruz, California, USA

May 3-7, 2009

Call for Papers

The **IEEE VLSI Test Symposium (VTS)** explores emerging trends and novel concepts in testing, and verification & validation of microelectronic circuits and systems. Major topics include, but are not limited to:

- Analog, M-S & RF Test
- ATE Architecture & SW
- Automatic Test Generation
- Board & System Test
- Biomedical Devices Test
- Built-In Self-Test (BIST)
- Current Based Test
- Defect Tolerance
- Delay & Performance Test
- Design for Testability (DFT)
- Design Verification/Validation
- Diagnosis and Debug
- Fault Modeling and Simulation
- FPGA Test
- High-Speed I/O Test
- Infrastructure IP
- MEMS Test
- Memory Test and Repair
- Microprocessor Test
- Nanometer Technologies Test
- On-Line Test
- Power Issues in Test
- Self-Repair & Fault Tolerance
- Sensor, MEMS, Microsystem Test
- SOC and SiP Test
- Standards
- System/Embedded System Test
- Test Economics
- Test Data Compression
- Test Quality and Reliability
- Test Resource Partitioning
- Thermal Test
- 3D System Test
- Transients and Soft Errors
- Yield Analysis & Optimization

The VTS Program Committee invites **original, unpublished paper submissions** for VTS 2009. Paper submissions should be complete manuscripts, up to six pages (inclusive of figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. A 50-word abstract and five keywords identifying the topic area are also required.

Proposals for the **Innovative Practices track**, and **Special Sessions** are also invited. The innovative practices track will highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. Special sessions can include panels, embedded tutorials, or hot topic presentations. Innovative practices track and special session proposals should include a title, name and contact information of the session organizer(s), a 150-to-200 word abstract, and a list of prospective participants.

All submissions are to be made electronically through the VTS website. **The EXTENDED DEADLINE for ALL submissions is November 9th 2008, 10PM GMT+1**. Detailed instructions for submissions are to be found at the conference website <http://www.tttc-vts.org>. Authors will be notified of the disposition of their papers by 9th January 2009. A submission will be considered as evidence that, upon acceptance, the author(s) will present the paper at the symposium, and will submit a final camera-ready version of the paper for inclusion in the proceedings. In the case of innovative practice and special sessions, the organizers commit to submit a session title, abstract, and list of participants for inclusion in the symposium proceedings and program.

VTS 2009 will present a **Best Paper Award**, a **Best Panel Award**, and a **Best IP Track Session Award** based on the evaluations of reviewers, attendees, and an invited panel of judges.

TTTC Test Technology Educational Program (TTEP) tutorials on emerging test technology topics will be offered during VTS 2009. Tutorial proposals should be submitted according to TTEP 2009 submission deadlines (<http://computer.org/tab/ttc/teg/ttep>).

VTS 2009 is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society. For more information on the VTS 2009 Test Event, visit the VTS website at <http://www.ttc-vts.org> or contact:

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