Technical Program

27th IEEE

VLSI TEST SYMPOSIUM

(VTS 2009)

Santa Cruz, CA, USA
3-6 May 2009

tttc™

IEEE

IEEE COMPUTER SOCIETY

27th IEEE VLSI TEST SYMPOSIUM
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C.J. Wu - *National Tsinghua U*
H. Wunderlich - *U Stuttgart*

27th IEEE VLSI TEST SYMPOSIUM (VTS 2009)

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27th IEEE VLSI TEST SYMPOSIUM VTS 2009
May 3rd - May 6th 2009
Santa Cruz, CA, USA
Welcome Message

Welcome to VTS 2009, the twenty-seventh in a series of annual symposia that focus on innovation in the field of testing of integrated circuits and systems.

The core of VTS 2009, the three day technical program, responds to the many trends and challenges in the semiconductor design and manufacturing industries with papers covering a diverse and seminal set of topics including, Fault Models, Transistor Aging and Power Supply Noise, Signal Integrity, Robust Design and Fault Tolerance, Radiation Test, Delay Fault Testing, Analog Test and Calibration, BIST, Microprocessor Test, Verification, Test Compaction, Debug, Diagnosis, Yield, Emergent Technology and Security.

In addition to the three-day technical program, VTS 2009 features several special sessions including several panels addressing various hot topics, two new topic speakers, and two student activity sessions. VTS 2009 continue the tradition of featuring the Innovative Practices track. The sessions that make up this track highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. This year the Workshop on Test of Wireless Circuits and Systems will take place in conjunction with VTS for the second year.

Two tutorials are offered by the TTTC Tutorials & Education Group through the Test Technology Education Program (TTEP). This year the tutorials cover the exciting topics of Statistical Testing and Silicon Debug and Diagnosis. The tutorials provide opportunities for design and test professionals to update their knowledge base in test, and earn official IEEE TTTC accreditation.

The social program at VTS provides an opportunity for informal technical discussions among participants. Santa Cruz, with its beaches and mountains, provides a very attractive backdrop for all VTS 2009 activities.

27th IEEE VLSI TEST SYMPOSIUM VTS 2009
May 3rd - May 6th 2009
Santa Cruz, CA, USA
Welcome Message

VTS is the result of the work of many dedicated volunteers: the reviewers, the best paper award judges, the Program Committee, the Organizing Committee, and the Steering Committee. We wholeheartedly thank them all. We also wish to thank all the authors who submitted their works to VTS 2009, and the program participants for their contribution at the symposium. We thank the IEEE Computer Society Test Technology Technical Council for its continued sponsorship and support. Finally, we thank the Corporate Supporters of VTS 2009.

We hope that you will find VTS 2009 enlightening, thought-provoking, rewarding, and enjoyable. We wish you all a fun-filled and productive week in the Santa Cruz area and hope that you will keep making VTS a success by actively participating in it, assisting in its organization, and letting us always know when we can do something better. Thank you all for coming.

General Chair
Magdy Abadir

Program Chair
Cecilia Metra

27th IEEE VLSI TEST SYMPOSIUM
Official Sponsors

The IEEE VLSI TEST SYMPOSIUM is sponsored by the IEEE COMPUTER SOCIETY'S Test Technology Technical Council (TTTC)

The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members' professional

development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology. TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters, and electronic broadcasts. All its activities are led by volunteer members. TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level.You may enroll as TTTC member for 2009 (no dues or fees) by using the embedded VTS 2009 Registration Form. To learn more about TTTC offerings and membership benefits, please visit:

http://tab.computer.org/tttc

27th IEEE VLSI TEST SYMPOSIUM
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27th IEEE VLSI TEST SYMPOSIUM
GENERAL INFORMATION
REGISTRATION

The IEEE VLSI Test Symposium explores emerging trends and novel concepts in the testing of integrated circuits and systems. The symposium is a leading international forum where many of the world's leading test experts and professionals from both industry and academia join to present and debate key issues in testing. VTS 2009 addresses key trends and challenges in the semiconductor design and manufacturing industries through an exciting program that includes Keynote and Plenary Talks, Technical Paper Sessions, Embedded Tutorial, Panels, Hot Topic Sessions, Full-day Tutorials, co-located Workshop, and the Innovative Practices Track.

Symposium Registration

VTS 2009 May 4th to 6th	**Advance Rate** (Until April 24, 2009)	**On-site Rate** (After April 24, 2009)
IEEE/CS Member Registration (Member rates are available only to current members of IEEE/CS. Please enter your valid membership number in order to qualify!)	**$525.00**	**$630.00**
Non-Member Registration	**$660.00**	**$800.00**
Student, Lifetime/Retired Registration (Valid student ID may be required at onsite registration check-in.)	**$225.00**	**$275.00**
Student Non-Member Registration	**$325.00**	**$375.00**
Additional Social Ticket (One Social Ticket is included for those paying IEEE/CS Member or Non-Member VTS rates. Students and companions of registered attendees must purchase a ticket to participate in the social event)	**$100.00**	**$100.00**

27th IEEE VLSI TEST SYMPOSIUM
GENERAL INFORMATION
REGISTRATION

Workshop Registration

WTW 2009 May 3rd	**Advance Rate** (Until April 24, 2009)	**On-site Rate** (After April 24, 2009)
IEEE/CS Member Registration (Member rates are available only to current members of IEEE/CS. Please enter your valid membership number in order to qualify!)	**$220.00**	**$275.00**
Non-Member Registration	**$275.00**	**$345.00**
Student, Lifetime/Retired Registration (Valid student ID may be required at onsite registration check-in.)	**$115.00**	**$175.00**
Half Day Member Registration	**$150.00**	**$225.00**
Half Day Non-Member Registration	**$190.00**	**$290.00**

TTEP Tutorials Registration

Tutorial No. 1 - May 3rd **Tutorial No. 2 - May 3rd**	**Advance Rate** (Until April 24, 2009)	**On-site Rate** (After April 24, 2009)
IEEE/CS Member Registration (Member rates are available only to current members of IEEE/CS. Please enter your valid membership number in order to qualify!)	**$320.00**	**$385.00**
Non-Member Registration	**$400.00**	**$480.00**

27th IEEE VLSI TEST SYMPOSIUM
GENERAL INFORMATION
LOCATION/ TRAVEL INFO

Location:

The City of Santa Cruz, California, is situated on the northern part of Monterey Bay about 74 miles south of San Francisco and 30 miles from San Jose. Santa Cruz is the county seat for the County of Santa Cruz.The City has of an area of 12 square miles.
For more information log on to :
http://www.ci.santa-cruz.ca.us/

About Seascape Beach Resort

Located just south of Santa Cruz, Seascape Beach Resort offers 285 luxurious suites and villas overlooking the Monterey Bay. You'll find all the comforts of home, plus the services and amenities of a four-diamond resort. Do anything you like or do nothing at all. With 17 miles of private beach, fine dining, and a full range of activities to choose from, Seascape Beach Resort has everything you need to make your experience memorable.

The resort is 30 miles away from San Jose Airport.

To contact the hotel:
Seascape Resort
One Seascape Resort Dr.
Aptos, CA 95003
831-662-7126 (Phone)
831-685-3059 (FAX)

The reservation cut-off date shall be 4th April 2009 at 5:00 p.m. Pacific time. Reservations received after this date will be accepted by the Hotel on a space available basis at the conference rates. Modifications made to existing reservations after this date will be treated as advance reservations.

Group rate

Deluxe Suite	$ 193.00
One Bedroom Beach Villa	$ 208.00
Two Bedroom Beach Villa	$ 347.00

The Group Rate covers all guest sleeping room costs, including service fees, and applicable sales/room tax (10%). All the following amenities are also included:

- High-speed internet access in beach villas, studios, suites and select public areas.
- Use of Fitness Center and Swimming Pool at Seascape Sports Club.
- All housekeeping and bell staff gratuities.
- Transportation throughout the resort.

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Monday, May 4th, 2009

09:00AM - 11:00AM
Seascape Grand Ballroom

PLENARY SESSION

Welcome Message:
Magdy Abadir, General Chair

Program Introduction:
Cecilia Metra, Program Chair

Keynote Speaker:
J. Kibarian, CEO and President of PDF Solutions

Invited Keynote:
Testing New Generation of Multifunctional Embedded Microsystems
B. Kaminska - Canadian Research Chair, Simon Fraser U

Awards presentation:
IEEE Fellow Awards
TTTC Most Successful Technical Meeting Award
TTTC Most Populous Technical Meeting Award
VTS 2008 Best Paper Award
VTS 2008 Best Panel Award
VTS 2008 Best Innovative Practices Award

11:00AM - 11:30AM BREAK

11:30AM - 12:30PM
Del Mar

Session 1A: **MICROPROCESSOR TEST**
Moderator: F. Lombardi - Northeastern U

1A.1 *Efficient Array Characterization in the UltraSPARC T2*
T. Ziaja, P. Tan - Sun MicroSystems Inc.

1A.2 *Instruction-Level Impact Comparison of RT- vs. Gate-Level Faults in a Modern Microprocessor Controller*
M. Maniatakos, Y. Makris - Yale U, N. Karimi - U of Tehran, C. Tirumurti, A. Jas - Intel

1A.3 *Modeling and Testing Comparison Faults of TCAMs with Asymmetric Cells*
J. F. Li, Y. J. Huang, Y. J. Hu - National Central U

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Monday, May 4th, 2009

11:30AM - 12:30PM
Pacific

Session 1B: **FAULT MODELS**
Moderator: H. J. Wunderlich - Stuttgart U

1B.1 *An Electrical Model for the Fault Simulation of Small-Delay Faults Caused by Crosstalk Aggravated Resistive Short Defects*
N. Houarche, M. Renovell - LIRMM, A. Czutro, P. Engelke, I. Polian, B. Becker - U Freiburg, M. Comte - U of Montpellier

1B.2 *Small Delay Fault Model for Intra-Gate Resistive Open Defects*
M. Arai, A. Suto, K. Iwasaki - Tokyo Metropolitan U, K. Nakano, M. Shintani, K. Hatayama, T. Aikyo - STARC

1B.3 *Defect Detection Differences between Launch-Off-Shift and Launch-Off-Capture in Sense-Amplifier-Based Flip Flop Testing*
H. Konuk - Broadcom

11:30AM - 12:30PM
Riviera

IP Session 1C: **DESIGN AND TEST PRACTICES AND TRENDS IN EAST ASIA**
Organizer: C. W. Wu - National Tsinghua U
Moderator: W. H. Wang - Intel

1C.1 *Design and Test Practices and Trends, from the Perspective of FTC*
H. P. Lin - Faraday

1C.2 *Design and Test Practices and Trends, from the Perspective of GUC*
J. Lai - Global Unichip

1C.3 *Design and Test Practices and Trends, from the Perspective of Richtek*
K. C. Chang - Richtek Technology

12:30PM - 02:15PM LUNCH*

*TTTC Service Awards presentation ceremony will take place at lunch venue between 01:00PM - 02:15PM

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Monday, May 4th, 2009

02:15PM - 03:15PM
Del Mar

Session 2A: **ROBUST DESIGN AND FAULT TOLERANCE**
Moderator: P. Prinetto - Polit di Torino

2A.1 *Soft-Error Hardening Designs of Nanoscale CMOS Latches*
S. Lin, Y. B. Kim, F. Lombardi - Northeastern U

2A.2 *Exploiting Unused Spare Columns to Improve Memory ECC*
R. Datta, N. Touba - U of Texas at Austin

2A.3 *An Adaptive-Rate Error Correction Scheme for NAND Flash Memory*
T. H. Chen, Y. Y. Hsiao, Y. T. Hsing, C. W. Wu - National Tsinghua U

02:15PM - 03:15PM
Pacific

Session 2B: **DELAY FAULT TESTING I**
Moderator: V. Agrawal - Auburn U

2B.1 *Compact Delay Test Generation with a Realistic Low Cost Fault Coverage Metric*
Z. Wang, D. M. H. Walker - Texas A&M U

2B.2 *Recursive Path Selection For Delay Fault Testing*
J. Chung, J. Abraham - U of Texas at Austin

2B.3 *A Synthesis Method to Alleviate Over-testing of Delay Faults Based on RTL Don't Care Path Identification*
Y. Yoshikawa, T. Inoue - Hiroshima City U,
S. Ohtake, H. Fujiwara - NIST

02:15PM - 03:15PM
Riviera

IP Session 2C: **ATE VISION 2020: NEW FRONTIERS FOR ATEs**
Organizer / Moderator: A. Koche - Verigy

2C.1 *Test Challenges of Device Scaling*
R. Barth - ITRS

2C.2 *The ATE Inside*
A. Crouch - Asset-Intertech

2C.3 *Getting the Inside Story*
C. Ritchie - Verigy

Innovative Practice Sessions

03:15PM - 03:45PM BREAK

03:45PM - 04:45PM
Del Mar

Session 3A: **DEBUG**
Moderator: Z. Navabi - Northeastern U

3A.1 *Automated Selection of Signals to Observe for Efficient Silicon Debug*
J. S. Yang, N. Touba - U of Texas at Austin

3A.2 *A New Post-silicon Debug Approach Based on Suspect Window*
G. Jianliang - *ICT,* X. Li, Y. Han - Chinese Academy of Sciences

3A.3 *Debug of Speed Path Failures Using Functional Tests*
S. Venkataraman, R. McLaughlin - Intel

03:45PM - 04:45PM
Pacific

Session 3B: **DELAY FAULT TESTING II**
Moderator: M. Breuer - U of Southern California

3B.1 *Output Hazard-Free Transition Delay Fault Test Generation*
S. Menon - AMD, A. Singh, V. Agrawal - Auburn U

3B.2 *Efficient Scheduling of Path Delay Tests for Latch-Based Circuits*
K. Y. Chung - Samsung, S. Gupta - U of Southern California

3B.3 *Effective and Efficient Test Pattern Generation for Small Delay Defects*
S. Goel, N. D. Prasanna, R. Turakhia - LSI Corp.

03:45PM - 04:45PM
Rivera

IP Session 3C: **INDUSTRIAL APPROACHES FOR QUALITY AND COMPRESSION**
Organizer: Y. Sato - Kyushu Institute of Tech.
Moderator: M. Arai - Tokyo Metropolitan U

3C.1 *Test Quality Improvement with Synchronized On-Chip Clocking*
Y. Onozaki, T. Hasegawa, S. Fujita - Toshiba
D. Martin, T. Ayres - Synopsys

Innovative Practice Sessions

3C.2 *Harmonious BIST: A DFT Approach to Higher Test Coverage and Higher Compression Ratio*
M. Sato, T. Hasegawa, K. Tsutsumida, Y. Sato - Hitachi, V. Chickermane, A. Uzzaman, P. Zhang - Cadence

3C.3 *Logic Depth, Test data Volume & Defects Per Million (DPM): A case study of Ultrasparc T2 SoC Multi-core Microprocessors*
P. Mantri, M. Gala - Sun Micro.

08:00PM - 09:30PM
Del Mar

Special Session 4A: **PANEL: APPRENTICE – VTS EDITION: SEASON 2**
Organizer / Moderator - K. S. Kim - Intel
Panelists:
A. Crouch - Asset-Intertech
A. Gattiker - IBM
S. Ozev - Arizona State U
B. Cory - NVidia
R. Kapur - Synopsys

08:00PM - 09:30PM
Pacific

Special Session 4B: **PANEL: DFT AND TEST PROBLEMS FROM THE TRENCHES**
Organizer / Moderator - H. Konuk - *Broadcom Corp.*
Panelists:
Z. Conroy - Cisco
B. Corey - NVidia
R. Aitken - ARM

08:00PM - 09:30PM
Riviera

Special Session 4C: **STUDENT POSTERS**
Organizers: Y. Makris - Yale U, H. Stratigopoulos - TIMA
Moderator: H. Stratigopoulos - TIMA

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Tuesday May 5th, 2009

08:30AM-09:30AM
Del Mar

Session 5A: **DIAGNOSIS**
Moderator: J. Ferguson, U of California, Santa Cruz

5A.1 *Multiple-Fault Silicon Diagnosis Using Faulty-Region Identification*
M. J. Tasi, C. T. Chao, J. Y. Jou, M. C. Wu - National Chiao Tung U

5A.2 *Predictive Test Technique for Diagnosis of RF CMOS Receivers*
K. Suenaga, R. Picos, S. Bota, E. Isern, E.G. Moreno, M. Roca -U of Balearic Islands

5A.3 *Controlling DPPM through Volume Diagnosis*
X. Yu, Y. T. Lin, R. S. Blanton - Carnegie Mellon U

08:30AM - 09:30AM
Pacific

Session 5B: **DELAY FAULT TESTING AND SIGNAL INTEGRITY**
Moderator: X. Li - *Chinese Academy of Sciences*

5B.1 *Scalable Compact Test Pattern Generation for Path Delay Faults Based on Functions*
E. Flanigan, S. Tragoudas, A. A. Rahman - Southern Illinois U

5B.2 *A Novel Test Application Scheme for High Transition Fault Coverage and Low Test Cost*
Z. Chen, D. Xiang, B. Yin - Tsinghua U

5B.3 *A High-Level Signal Integrity Fault Model and Test Methodology for Long On-Chip Interconnections*
S. Chun, Y. Kim, T. Kim, S. Kang - Yonsei U

08:30AM - 09:30AM
Riviera

IP Session 5C: **YIELD AND MARGINALITIES**
Organizer / Moderator: R. Aitken - ARM

5C.1 *Trading Off Margin vs. Yield: Is What We Model What We Get?*
A. Gattiker - IBM

5C.2 *Process Variability-Induced Timing Failures*
C. E. Lew - Qualcomm

5C.3 *Can You Blame System Fails On Low Margin?*
Z. Conroy - Cisco

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Tuesday May 5th, 2009

09:30AM - 10:00AM BREAK

10:00AM - 11:00AM

Del Mar

Session 6A: **Yield**
Moderator: S. Bernard - LIRMM

6A.1 *False Path Aware Timing Yield Estimation Under Variability*
L. Xie, A. Davoodi, K. Saluja, A. Sinkar - U of Wisconsin Madison

6A.2 *Bridging DFM Analysis and Volume Diagnostics for Yield Learning*
M. Ward, S. Goel, R Turakhia - LSI Corp.
B. Benware - Mentor Graphics

6A.3 *Yield and Cost Analysis of a Reliable NoC*
S. Shamshiri, K. T. Cheng - UCSB

10:00AM - 11:00AM

Pacific

Session 6B**: BIST**
Moderator: S. Hellebrand - U of Paderborn

6B.1 *Restrict Encoding for Mixed-Mode BIST*
A. W. Hakmi, S. Holst, H. J. Wunderlich - U of Stuttgart, J. Schlöffel, F. Hapke, A.Glowatz - Mentor Graphics

6B.2 *A Scalable, Digital BIST Circuit for Measurement and Compensation of Static Phase Offset*
K. Jenkins, L. Li - IBM TJ Watson Research Center

6B.3 *Experimental Validation of a BIST Technique for CMOS Active Pixel Sensors*
L. Lizarraga, S. Mir, G. Sicard - TIMA

10:00AM - 11:00AM

Riviera

IP Session 6C: **NEW PRACTICES IN DEFECT-BASED TESTING**
Organizer / Moderator: P. Maxwell - Aptina

6C.1 *Test for Reliability of Embedded SRAM*
P.K. Ahuja - Sun Microsystems

6C.2 *Marginal Defects: Are Power-Only Defects Really Defects?*
J. Fitzgerald - AMD

6C.3 *T.B.D.*
H. Manhaeve - QStar

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Tuesday May 5th, 2009

11:00AM - 11:30AM BREAK

11:30AM-12:30PM

Del Mar

Session 7A: **TEST AND VERIFICATION**
Moderator: S. Davidson - Sun Micro.

7A.1 *Physically-Aware N-Detect Test Relaxation*
Y. T. Lin, C. Ezekwe, R.S. Blanton - Carnegie Mellon U

7A.2 *Automatic Selection of Internal Observation Signals for Design Verification*
T. Lu - Institute of Computing Technology, H. Li, X. Li - Chinese Academy of Sciences

7A.3 S*TDF Memory Fail Datalog Standard*
A. Khoche - Verigy

11:30AM-12:30PM

Pacific

Session 7B: **TRANSISTOR AGING AND POWER SUPPLY NOISE**
Moderator: H. Manhaeve - Qstar

7B.1 *Test Patterns for Transistor Aging*
A. H. Baba, S. Mitra - Stanford U

7B.2 *Layout-Aware Pattern Generation for Maximizing Supply Noise Effects on Critical Paths*
J. Ma, J. Lee, M.Tehranipoor - U of Connecticut

7B.3 *Understanding Power Supply Droop During At-Speed Scan Testing*
P. Pant, J. Zelman - Intel

11:30AM-12:30PM

Riviera

IP Session 7C: **VALUE OF DFM IN VOLUME DIAGNOSIS ARENA**

Organizers: S. K. Goel, M. Ward - LSI Corp.
Moderator: G. Eide - Mentor Graphics

7C.1 *Automation in Silicon Characterization*
R. Aitken - ARM

7C.2 *Using Volume Diagnostics and DFM Practices to Drive Yield Improvement*
M. Ward - LSI

7C.3 *Tying DFM to Test and Volume Diagnosis*
S. Venkataraman - Intel

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Tuesday May 5th, 2009

12:30PM - 01:30PM LUNCH

01:30PM - 03:00PM

Riviera

Special Session 8A: **NEW TOPIC: AT-SPEED TESTING IN THE FACE OF PROCESS VARIATIONS**
Organizer: B. Courtois - TIMA
Moderator: X. Gu - Cisco
Presenter: C. Visweswariah - IBM

01:30PM - 03:00PM

Pacific

Special Session 8B: **TTTC 2009 BEST DOCTORAL THESIS CONTEST**

Organizers: Y. Makris - Yale U
H. Stratigopoulos - TIMA.
Moderator: H. Stratigopoulos - TIMA.

01:30PM - 03:00PM

Del Mar

Special Session 8C: **Apprentice Panel Judging Session**
Moderator: K. S. Kim - Intel

03:30PM - 10:00PM

SOCIAL PROGRAM

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Wednesday May 6th, 2009

08:30AM - 09:30AM

Riviera

Special Session 9A: **NEW TOPIC: MICROSCALE AND NANOSCALE THERMAL CHARACTERIZATION OF INTEGRATED CIRCUIT CHIPS**
Organizer: B. Courtois - TIMA
Moderator: X. Gu - CISCO
Presenter: A. Shakouri - U of California, Santa Cruz

08:30AM - 09:30AM

Pacific

Special Session 9B: **EMBEDDED TUTORIAL: QUANTUM WIRES, QUANTUM WIRE ARRAYS: WHAT ARE THEY ? WHY IS ANYONE INTERESTED? AND HOW DO YOU KNOW YOU HAVE ONE?**
Moderator: J. Abraham - U of Texas at Austin
Presenter: A. Sacco - Northeastern U

09:00AM - 10:00AM BREAK

10:00AM - 11:00AM

Del Mar

Session 10A: **TEST COMPACTION**
Moderator: C. J. Clark - Intellitech Corp.

10A.1 *Highly X-Tolerant Selective Compaction of Test Responses*
J. Tyszer, D. Czysz - Poznan U, G. Mrugalski, N. Mukherjee, J. Rajski - Mentor Graphics

10A.2 *Dynamic Test Compaction for Transition Faults in Broadside Scan Testing Based on an Influence Cone Measure*
D. Xiang, B. Yin - Tsinghua U, K.-T. Cheng, Z. Chen - UCSB

10A.3 *Maintaining Accuracy of Test Compaction through Adaptive Modeling*
S. Biswas, R. S. Blanton - Carnegie Mellon U

10:00AM - 11:00AM

Pacific

Session 10B: **TEST AND RADIATION TEST**
Moderator: P. Varma - Blue Pearl

10B.1 *RT-Level Deviation-Based Grading of Functional Test Sequences*
H. Fang, K. Chakrabarty - Duke U, A. Jas, S. Patil, C.Tirumurti - Intel

10B.2 *Analytical Model for Multi-site Efficiency with Clustering, Yield and Parallel to Serial Test Times*
R. Daasch, N Velamati - Portland State U

10B.3 *DFT Reuse for Low-Cost Radiation Testing of SoCs: a case study*
P. Bernardi, M. Grosso, M. Sonza Reorda - Polit Di Torino, P. Rech, S Gerardin, A.Paccagnella - U di Padova, D. Appello - ST Microelectronics

10:00AM - 11:00AM

Riviera

IP Session 10C: **DFT AND TEST PRACTICES FOR POWER-MANAGED LOW POWER CHIPS**

Organizers/Moderators: S. Ravi - Texas Instruments, K. Hatayama - STARC

10C.1 *Manufacturing Test and Silicon Debug Practices for Power Managed Chips*
S. Ravi , A. Bhat - Texas Instruments

10C.2 *An EDA Perspective on Power Management Test*
V. Chickermane - Cadence

10C.3 *The Application of CooLBIST for a Real Chip*
H. Iwata, J. Matsushima, Y. Maeda, M. Takakura - Renesas

11:00AM - 11:30AM BREAK

Innovative Practice Sessions

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Wednesday May 6th, 2009

11:30PM - 01:00PM
Del Mar

Session 11A: **ANALOG TEST AND CALIBRATION**
Moderator: A. Ivanov - U of British Columbia

11A.1 *On-line Calibration and Power Optimization of RF Systems Using a Built-in Detector*
C. Zhang, R. Gharpurey, J. Abraham - U of Texas at Austin

11A.2 *Calibration and Testing Time Reduction Techniques for a Digitally-Calibrated Pipelined ADC*
H. M. Chang, C. H. Chen, K. T. Cheng - UCSB
K. Y. Lin - Industrial Technology Research Institute

11A.3 *A Time Domain Method to Measure Oscillator Phase Noise*
K. Blakkan - Cypress Semiconductor, M. Soma - U of Washington

11A.4 *A Packet Based 2-Site Test Solution for GSM Transceivers with Limited Tester Resources*
E. Erdogan - Duke U, S. Ozev - Arizona State U

11:30PM - 01:00PM
Pacific

Session 11B: **EMERGENT TECHNOLOGY AND SECURITY**
Moderator: J. Tyszer - Poznan U

11B.1 *Design-for-Testability for Digital Microfluidic Biochips*
T. Xu, K. Chakrabarty - Duke U

11B.2 *Stuck-Open Fault Leakage and Testing in Nanometer Technologies*
V. H. Champac, J. Vazquez Hernandez - INAOE, C. Hawkins - U New Mexico, J. Segura - U des Illes Ballears

11B.3 *SS-KTC: A High-Testability Low-Overhead Scan Architecture with Multi-Level Security Integration*
D. Zhao, U. Chandran - U of Louisiana

11B.4 *Characterization of Effective Laser Spots during Attacks in the Configuration of a Virtex-II FPGA*
G. Canivet, R. Leveugle - TIMA, J. Clédières - CEA/LETI, F. Valette - DGA/CELAR, M. Renaudin - TIEMPO

01:00PM - 02:00PM LUNCH

27th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM AGENDA
Wednesday May 6th, 2009

02:00PM - 03:30PM
Riviera

Special Session 12A: **PANEL: ANALOG TEST AND CHARACTERIZATION: THE LONG ROAD TO REALIZATION**
Organizer: A. Sinha - AMD
Moderator: V.Ganti - AMD
Panelists:
G. Roberts - McGill U
J. Macri - AMD
M. D'Abreau - Sandisk
S. Sunter - Logic Vision

02:00PM - 03:30PM
Pacific

Special Session 12B: **PANEL: SOC POWER MANAGEMENT IMPLICATIONS ON VALIDATION AND TESTING**
Organizer: B. Kapoor - MIMASIC
Moderator: S. Tabatabaei - SiTime
Panelists:
B. Kapoor - MIMASIC
S. Hemmady - Synopsys
S.Verma - Conexant

27th IEEE VLSI TEST SYMPOSIUM
SOCIAL PROGRAM

For this year's social event, we will start at 3:30 PM by taking a bus ride to explore the beautiful California scenery. A trip in California is not complete without a stop at one of its legendary wineries. This year we will visit the Fortino Winery close to the city of Gilroy. You will get to network and socialize while enjoying wine-tasting and a tour of the winery. Buses will return back to the resort to arrive around 7PM.

Once we are back at the resort, we will head to the beach! Dinner will be served on the beautiful beach of the Seascape resort. Dinner festivities will start at 7PM and lasts until 10PM. You will get to enjoy great food and drinks at the beachside accompanied by beautiful California sunset.
A fire will be setup as it gets dark into the night. You can continue to enjoy the sounds of the ocean alongside the fire or take a walk on the beach after dinner. Just remember to dress warm as the sea breeze can be a bit cold.

There is no extra cost for this program for VTS attendees who register at member and non-member rates. Students and companions of VTS attendees can register for the Social Program for $100 per person. So, come and join us!

Useful information:
Fortino Winery
4525 Hecker Pass Hwy
Gilroy, CA 95020

27th IEEE VLSI TEST SYMPOSIUM
TEST TECHNOLOGY
EDUCATIONAL PROGRAM 2009

The Tutorials and Education Group of TTTC continues the organization of a comprehensive set of test technology tutorials. These comprise tutorials in conjunction with TTTC sponsored technical meetings, web-based tutorials, and on-site tutorials and courses. The tutorials are part of the successful annual Test Technology Educational Program (TTEP 2009).

TTEP intends to serve both test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics and also the opportunity to earn official certification from IEEE TTTC. Each six-hour tutorial corresponds to four TTEP units. Upon completion of each sixteen TTEP units official accreditation in the form of an "IEEE TTTC Test Technology Certificate" is presented to the participants.

For further information

Dimitris Gizopoulos
Tutorials and Education Group Chair
University of Piraeus, Greece
Tel: +30 210 414 2372
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TTEP web site: http://tab.computer.org/tttc/teg/ttep

27th IEEE VLSI TEST SYMPOSIUM
TUTORIAL 1
Sunday, May 3rd 2009

8:30AM -4:30PM

Tutorial: Advanced Topics and Recent Advances in Silicon Debug and Diagnosis

PRESENTERS: S. Venkataraman (Intel),
M.Abramovici,
R. Aitken (ARM)

AUDIENCE: IC Designers; test, DFT, and product engineers; DA developers; validation, debug, and failure analysis engineers; researchers, managers, and anyone else determined to shorten the time-to-volume of a newly manufactured chip

DESCRIPTION: The increasing design complexity along with the emergence of new failure mechanisms in the nanometer regime has significantly increased the complexity of verification, validation and manufacturing ramp of ICs. When pre-silicon verification and validation uncovers design bugs, the process of diagnosing and debugging these issues is called design error diagnosis. From the time a new chip comes back from the fab until high-volume production can start, the chip goes through functional silicon validation and debug to make sure it is free of design errors, and defect diagnosis and failure analysis to solve yield problems. These activities, referred to as silicon debug and diagnosis, have become the most time-consuming phase in the development cycle of a new design, increasing to about one third of the total time. This is a consequence of the increasing design complexity, along with the emergence of new failure mechanisms in nanometer technologies. Long time-to-volume and low manufacturing yield have a great detrimental impact on the economic viability and the overall success of a product. This tutorial covers the state of the art and the full spectrum of topics in silicon validation and debug and defect diagnosis ranging from the basic concepts to advanced applications and new DFD techniques. It also describes successful debug and diagnosis methods used in real industrial products, industrial experiences, and case studies, as well as future directions and challenges.

27th IEEE VLSI TEST SYMPOSIUM
TUTORIAL 2
Sunday, May 3rd 2009

8:30AM -4:30PM

Tutorial: Statistical Adaptive Test Methods Targeting "Zero Defect" IC Quality and Reliability

PRESENTERS: : A. Singh (Auburn University)

AUDIENCE: Test and Reliability Engineers, Engineering Managers, Reliability and Quality Assurance Managers, Researchers and Research Students

DESCRIPTION: Integrated circuits have traditionally all been tested identically in the manufacturing flow. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by adaptively subjecting "suspect" parts to more extensive testing. The idea is similar to security screening at airports. Such methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production circuits from several companies.

IEEE Workshop on Test of Wireless Circuits and Systems WTW 2009

SCOPE: The Wireless Test Workshop (WTW) includes, among others, the following major topics in RF test: Case Studies, High-Frequency Test, Embedded RF Circuit Test, RF Test Board Related Issues, Yield Learning, Wireless Test Methodology, Standards Conformance Test, Noise Characterization and Validation, Economics of Test, Wireless Product Test Equipment and Metrology.

For this year, the program committee has put together an exciting and a highly technical program, this year main focus is on:

- Challenges and Opportunities in Next Generation RF Transceivers by an Intel Fellow
- 60GHz and beyond test challenges by CEO of Roos Instruments
- 4G test challenges
- Protocol aware HTOL
- System level vs. Parametric test what Strategies Provide the Lowest COT, Highest Quality, Best Yield, & Shortest Time to Volume

The workshop encourages discussion and the technical program is oriented to create an atmosphere that facilitates audience learning and contribution to the subject matter.

Advance Program Summary:

1. Keynote Speaker: Challenges and Opportunities in Next Generation RF Transceivers
2. Invited Speaker: mmWave ATE RFIC Production Test
3. Session #2: Min-Tutorial: LTE Test Challenges
4. Session #3: Panel: Modulation vs CW Test: What Strategies Provide the Lowest COT, Highest Quality, Best Yield, & Shortest Time to Volume?
5. Session #4: Advanced Test Techniques

REGISTRATION: All WTW 2009 participants require registration, which includes workshop technical sessions, workshop informal proceedings, break refreshments, and lunch.

SPONSORSHIP: WTW 2009 is sponsored by the IEEE Computer Society TTTC.

INFORMATION: For further details on the technical program, please contact Program Chair, Mustapha Slamani (slamanim@us.ibm.com). Regarding other questions, please contact the General Chair, Rob Aitken (rob.aitken@arm.com).

Please visit our web-site:
http://www.wtw2009.tec.ufl.edu/

27TH IEEE VLSI TEST SYMPOSIUM - PROGRAM AT A GLANCE

Sunday, May 3rd 2009			
07:30AM - 08:30AM	REGISTRATION		
08:30AM - 04:30PM	TUTORIAL 1 - Advanced Topics and recent Advances in debug and daignosis	TUTORIAL 2 - Statistical Adaptive Test Methods Targeting “Zero Defect" IC Quality and Reliability	
Monday, May 4rd 2009			
09:00AM - 11:00AM	PLENARY SESSION		
11:30AM - 12:30AM	Session 1A - Microprocessor Test	Session 1B: Fault Models	Session 1C: Design and Test Practices and Trends in East Asia
12:30PM - 02:15PM	LUNCH & TTTC Service Award Presentation		
02:15PM - 03:15PM	Session 2A: Robust Design and Fault Tolerance	Session 2B: Delay Fault Testing I	Session 2C: ATE Vision 2020: New Frontiers For ATEs
03:45PM - 04:45PM	Session 3A: Debug	Session 3B: Delay Fault Testing II	Session 3C: Industrial Approaches for Quality and Compression
08:00PM - 09:30PM	Session 4A: Panel: Apprentice - VTS Edition: Season 2	Session 4B: Panel: DFT and Test Problems from the Trenches	Session 4C: Student Posters
Tuesday, May 5th 2009			
08:30AM - 09:30 AM	Session 5A: Diagnosis	Session 5B: Delay Fault Testing and Signal Integrity	Session 5C: Yield and Marginalities

10:00AM - 11:00AM	Session 6A: Yield	Session 6B: BIST	Session 6C: New Pratices in Defect-Based Testing
11:30AM - 12:30PM	Session 7A: Test and Verification	Session 7B: Transistor Aging and Power Supply Noise	Session 7C: Value of DFM in Volume Diagnosis Arena
12:30PM - 01:30PM	LUNCH		
1:30PM - 3:00PM	Session 8A: New Topic - At Speed Testing in the Face of Process Variations	Session 8B: TTTC 2009 Best Doctoral Thesis Contest	Session 8C: Apprentice Panel Judging Session
03:30PM - 10:00PM	Social Program		
Wednesday, May 6th 2009			
08:30AM - 09:30AM	Session 9A: New Topic: Microscale and Nanoscale Thermal Characterization of Intergrated Circuit Chips	Session 9B: Embedded Tutorial: Quantum Wires, Quantum Wire Arrays:What are they ? Why is anyone interested ? And how do you know you have one ?	
10:00AM - 11:00AM	Session 10A: Test Compaction	Session 10B: Test and Radiation Test	Session 10C: DFT and Test Practices for Power-Managed Low Power Chips
11:30AM - 01:00PM	Session 11A: Analog Test and Calibration	Session 11B: Emergent Technology and Security	
01:00PM - 02:00PM	LUNCH		
02:00PM - 03:30PM	Session 12A: Panel: Analog Test and Characterization : The long Road to Realization	Session 12B: Panel: SOC Power Management Implications on Validation and Testing	

Innovative Practice Sessions *Special Sessions*

27th IEEE VLSI TEST SYMPOSIUM
FRINGE MEETINGS

A number of TTTC professional groups interested in test will hold their meetings at VTS 2009. At press time, the following meetings were scheduled. These meetings are for members. If you'd like to attend, please contact the person listed at the e-mail address given. Please check with VTS09 onsite registration desk for room locations.

MONDAY, May 4th	
*12:30 pm - 2:15 pm	**Test Week Workshop Coordination** Yervant Zorian (zorian@viragelogic.com)
2:00 pm - 3:00 pm	**TTTC Tutorials and Education Group** Dimitris Gizopoulos (dgizop@unipi.gr)
3:00 pm - 4:00 pm	**TTTC Executive Committee** Adit Singh (adsingh@eng.auburn.edu)
4:00 pm - 5:00 pm	**ITRS Test Open Meeting** Mike Rodgers (mjrodge2@sbcglobal.net)
5:00 pm - 6:00 pm	**TTTC Senior Leadership Board** Yervant Zorian (zorian@viragelogic.com)
**6:00 pm - 8:00 pm	**IEEE VTS Program Committee** Cecilia Metra (cecilia.metra@deis.unibo.it)
TUESDAY, May 5th	
8:00 am - 9:30 am	**TTTC Technical Meetings Review Committee** Chen-Huan Chiang (chenhuan@alcatel-lucent.com)
11:00 am - 12:00 pm	**ITRS DFT SubTeam** Yervant Zorian (zorian@viragelogic.com)
*12:30 pm - 1:30 pm	**TTTC Standards Group** Rohit Kapur (rohit.kapur@synopsys.com)
*12:30 pm - 1:30 pm	**Int'l OnLine Test Symposium Committee** Michael Nicolaidis (michael.nicolaidis@imag.fr)
2:00 pm - 3:00 pm	**TTTC Communications Group** Cecilia Metra (cecilia.metra@deis.unibo.it)
WEDNESDAY, May 6th	
8:00 am - 9:30 am	**TTTC Operations Committee** Adit Singh (adsingh@eng.auburn.edu)
11:00 am - 1:00 pm	**IEEE VTS Organizing Committee** Magdy Abadir (M.Abadir@freescale.com)
*1:00 pm - 2:00 pm	**TTTC Middle East and Africa Group** Rafic Makki (makki@uaeu.ac.ae)

**Meeting During Lunch Break*
***Meeting During Dinner*