Technical Program

26th IEEE

VLSI TEST SYMPOSIUM (VTS 2008)

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26th IEEE VLSI TEST SYMPOSIUM
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26th IEEE VLSI TEST SYMPOSIUM (VTS 2008)

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26th IEEE VLSI Test Symposium
VTS 2008
April 27- May 1, 2008
Rancho Bernardo Inn
San Diego, California, USA
INTRODUCTION

Welcome to VTS 2008, the twenty-sixth in a series of annual symposia that focus on innovation in the field of testing of integrated circuits and systems.

The core of VTS 2008, the three day technical program, responds to the many trends and challenges in the semiconductor design and manufacturing industries with papers covering a diverse and seminal set of topics including, RF, Analog and Mixed Signal Circuit Test, ATPG, Delay Test, High Speed Test, Memory Test, Memory Diagnosis and Repair, Compaction for Testing, Debug and Diagnosis, Modeling and Testing for Nanometer CMOS, SOC Test, Reliability in Nanoscale CMOS, Testing and Error Tolerance for Emergent Technology Circuits and Fault Tolerance.

In addition to the three-day technical program, VTS 2008 features special sessions, and the Innovative Practices track. These tracks highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. Full-day tutorials and workshops are also held in conjunction with VTS 2008. The workshops are the International Workshop on Silicon Debug and Diagnosis and the Workshop on Test of Wireless Circuits and Systems. Three tutorials are offered by the TTTC Tutorials & Education Group through the Test Technology Education Program (TTEP). The tutorials by leading VLSI test academics and practitioners provide introduction to a diverse set of topics, including reliability and hardening techniques, statistical screening, and analog, mixed-signal and RF circuit testing. The tutorials provide opportunities for design and test professionals to update their knowledge base in test, and earn official IEEE TTTC accreditation.

The social program at VTS provides an opportunity for informal technical discussions among participants. San Diego, California, provides a highly attractive backdrop for all VTS 2008 activities. For the first time, VTS will have an international social program to sample the charms of Baja California, Mexico.

INTRODUCTION (Continued)

VTS is the result of the work of many dedicated volunteers: the reviewers, the best paper award judges, the Program Committee, the Organizing Committee, and the Steering Committee. We wholeheartedly thank them all. We also wish to thank all the authors who submitted their research to VTS 2008, and the program participants for their contribution at the symposium. We thank the IEEE Computer Society Test Technology Technical Council for its continued sponsorship and support. And most importantly, we would like to offer a heartfelt word of thanks to all the Corporate Supporters of VTS 2008 who have contributed generously.

We hope that you will find VTS 2008 enlightening, thought-provoking, rewarding, and enjoyable. We wish you all a fun-filled and productive week in San Diego and hope that you will keep making VTS a success by actively participating in it, assisting in its organization, and letting us always know when we can do something better. Thank you all for coming.

Alex Orailoglu
General Chair

Peter Maxwell and **Cecilia Metra**
Program Co-Chairs

26th IEEE VLSI TEST SYMPOSIUM
Official Sponsors

The IEEE VLSI TEST SYMPOSIUM is sponsored by the IEEE COMPUTER SOCIETY'S Test Technology Technical Council (TTTC)

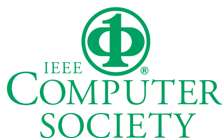
The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members' professional

development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology.

TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters, and electronic broadcasts. All its activities are led by volunteer members.

TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. You may enroll as TTTC member for 2008 (no dues or fees) by using the embedded VTS 2008 Registration Form. To learn more about TTTC offerings and membership benefits, please visit:

http://tab.computer.org/tttc



26th IEEE VLSI TEST SYMPOSIUM
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26th IEEE VLSI TEST SYMPOSIUM GENERAL INFORMATION

All activities require a registration badge for admittance. All participants must pay the appropriate fees. Reduced fees are available to IEEE or Computer Society members on presentation of a valid member number.

To register, use the Symposium Registration Form. To receive early registration discount rates, your completed Registration Form must be RECEIVED in the VTS office by mail or fax by April 11, 2008. Until April 11, you may register online at:

www.tttc-vts.org

After April 11, advance registration will no longer be available and you must register at the hotel at the higher rates listed in the table. After April 11, SPACE IS NOT GUARANTEED in the Social Program.

Technical program registration includes a copy of the Proceedings, the social program, three luncheons, three morning coffee services, and five coffee breaks. Student registration does not include the social program. Students and companions of registered attendees can buy tickets for the social program at $100 per person. Extra copies of the Proceedings are available at $50 each. Lunch tickets for companions of registered attendees will be available at the symposium ($45 each).

The Registration Form allows you to automatically enroll or renew your TTTC membership (no dues or fees) by checking the corresponding box.

The Wireless Test Workshop (WTW 2008) will take place April 27th from 8:30 am to 5:30 pm. Registration includes workshop technical sessions, workshop informal proceedings, break refreshments, and lunch.

The International Workshop on Silicon Debug and Diagnosis (SDD 2008) will take place April 30th from 4:00 pm to 6:00 pm, and May 1st from 8:00 am to 5:30 pm. Registration includes workshop technical sessions, workshop informal proceedings, reception dinner on April 30th, continental breakfast, break refreshments, and lunch.

Tutorial registration for members and non-members includes lecturer’s notes, breaks, and lunch.

26th IEEE VLSI TEST SYMPOSIUM GENERAL INFORMATION (Continued)

REGISTRATION FEES:

Early Registration*	IEEE/CS Member	Student Member	Student Non-Member	Non-Member
SYMPOSIUM	$525	$225	$325	$650
TUT. 1	$320	$320	$400	$400
TUT. 2 or 3	$320	$320	$400	$400
WTW	$220	$115	$150	$275
SDD	$275	$160	$200	$350

Registration At Hotel	IEEE/CS Member	Student Member	Student Non-Member	Non-Member
SYMPOSIUM	$630	$275	$375	$800
TUT. 1	$385	$385	$480	$480
TUT. 2 or 3	$385	$385	$480	$480
WTW	$275	$175	$225	$345
SDD	$325	$200	$240	$420

*Social Program Fee** $100*

**discounts available through April 11, 2008*
***for students and companions of registered attendees*

REFUNDS: If you must cancel, advance registration fees will be refunded only upon written request to: VLSI Test Symposium, 1474 Freeman Drive, Amissville, VA, 20106, USA postmarked on or before April 11, 2008. A $50 processing fee is charged for each refund.

26th IEEE VLSI TEST SYMPOSIUM TRAVEL INFORMATION

AIR

The San Diego International Airport serves the San Diego, CA area.

AIRPORT GROUND TRANSPORTATION

Cab fare from San Diego International Airport to The Rancho Bernardo Inn Golf Resort & Spa costs approximately $65/one way.

For additional information on the airport ground transportation, go to: http://www.san.org/airport/ground_transportation

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DIRECTIONS TO THE RANCHO BERNARDO INN GOLF RESORT AND SPA

From San Diego International Airport:

- Take Harbor Drive south (toward downtown)
- Turn left at Grape Street
- Go east to the top of the hill, then take Interstate 5 south
- Stay in the right lane and follow Route 163 north toward Escondido
- (Route 163 becomes Interstate 15)
- Take the Rancho Bernardo Road exit east to Pomerado Road (4th light)
- Turn left on Pomerado Road
- Turn left onto Greens East Road
- Follow the signs to the resort entrance

From Interstate 15:

- Take the Rancho Bernardo Road exit east to Pomerado Road (4th light)
- Turn left on Pomerado Road
- Turn left onto Greens East Road
- Follow the signs to the resort entrance

26th IEEE VLSI TEST SYMPOSIUM HOTEL INFORMATION

The 26th IEEE VLSI Test Symposium will be held at The Rancho Bernardo Inn Golf Resort & Spa in San Diego, CA. Rancho Bernardo Inn Golf Resort & Spa is one of San Diego's premier Golf Resorts close to everything that makes San Diego one of the nations most popular travel destinations; Southern California's famous Beaches, Wild Animal Park, SeaWorld, world-famous San Diego Zoo, LegoLand and more. Their recently completed $25 million-dollar renovation included completely refurbished Guest Accommodations with upgrades throughout including: 42" Flat-Screen TVs, Wireless Internet, Private Patios or Balconies, and more.

To contact the hotel:

Rancho Bernardo Inn Golf Resort & Spa
17550 Bernardo Oaks Drive
San Diego, CA 92128
Tel: +1-800-542-6096 (Toll Free) or
+1-858-675-8500
Fax: +1-858-675-8501
www.ranchobernardoinn.com

Phone Reservations

To reserve a room at the resort, please call The Rancho Bernardo Inn Golf Resort & Spa at +1-800-542-6096 referencing **IEEE** (VLSI Test Symposium) when making your reservations in order to receive the Symposium discount rate.

Online Reservations

Reservations can also be made online with
Group Code 2504CEM20 at the resort website:
www.ranchobernardoinn.com

The reservation cut-off date is Monday, April 7th, 5:00 PM Pacific time to obtain the special discount rate ($169.00 US) single/double, plus tax. After April 7th, 2008, reservations may be taken if space is available; however, rates may be higher.

To cancel a reservation and receive a refund, you must notify the resort by 6:00 p.m. on the date of your arrival.

26th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Monday, April 28th, 2008

9:00 am – 10:30 am

Aragon Ballroom II

PLENARY SESSION

Welcome Message:
Alex Orailoglu, General Chair

Keynote Speaker:
Michael Campbell, Senior Vice President of Engineering, Qualcomm CDMA Technologies

Program Introduction:
Peter Maxwell and Cecilia Metra**,** Program Co-Chairs

Invited Keynote:
"A Revolution in Design and Test Technology," Prof. Melvin Breuer, University of Southern California

Awards Presentation:
TTTC Most Successful Technical Meeting Award
TTTC Most Populous Technical Meeting Award
VTS 2007 Best Paper Award
VTS 2007 Best Panel Award
VTS 2007 Best Innovative Practices Award

10:30 am – 11:00 am BREAK

11:00 am – 12:00 pm

Aragon I

Session 1A: **TESTING FOR HIGH SPEED COMMUNICATION SYSTEMS**
Moderator: B. Courtois – TIMA

1A.1 *Low-Cost Test of Timing Mismatch Among Time-Interleaved A/D Converters In High-Speed Communication Systems,* Q. Dou, J. Abraham – Univ. of Texas at Austin

1A.2 *Test Enabled Process Tuning for Adaptive Baseband OFDM Processor,* M. Nisar, A. Chatterjee –Georgia Inst. of Tech.

1A.3 *Bit-Error Rate Estimation for Bang-Bang Clock and Data Recovery Circuit in High-Speed Serial Links,* D. Hong, K.T. Cheng – Univ. of California, Santa Barbara.

11:00 am – 12:00 pm

Aragon II

Session 1B: **COMPACTION FOR TESTING**
Moderator: T. Williams – Synopsys

1B.1 *How Many Test Patterns are Useless?,* F.F. Ferhani – Stanford Univ., N. Saxena – NVIDIA, E. McCluskey – Stanford CRC, P. Nigh – IBM

1B.2 *Constructing Augmented Multimode Compactors,* E. Gizdarski – Synopsys

1B.3 *Increasing Output Compaction in Presence of Unknowns using an X-Canceling MISR with Deterministic Fault Detection,* R. Garg, N. Touba – Univ. of Texas at Austin, R. Putman – Cirrus Logic

11:00 am – 12:00 pm

Aragon III Session 1C: **HIGHWAYS TO ZERO-DEFECTS: INDUSTRIAL APPROACHES**
Organizers: A. K. Majhi – NXP
Moderator: David Wu – Intel

1C.1 *DFT Opportunities to Achieve Zero Defects,* R. Raina, L. Winemberg – Freescale

1C.2 *Statistical Scan Diagnosis - New Road to High Quality,* S. Eichenberger, C. Hora, J. Geuzebroek, B. Kruseman, A. K. Majhi – NXP

1C.2 *Extending Quality Beyond Time Zero Through Additional DFT and Test,* S. K. Vooka, V. Jayaram, R. Parekhji – Texas Instruments

12:00 pm – 1:20 pm LUNCH

1:20 pm – 2:20 pm

Aragon I Session 2A: **ATE DATA VOLUME AND FALSE/ ACCEPTABLE TEST FAILS**
Moderator: E. Volkerink – Verigy

2A.1 *Inconsistent Fails Due to Limited Tester Timing Accuracy,* I. Park, D. Lee – Stanford Univ., E. Chmelar – LSI Logic, E. McCluskey - Stanford CRC

2A.2 *A Regression Based Technique for ATE-Aware Test Data Volume Estimation of System-on-Chips (SoCs),* S. Ravi, R. Tiwari, A. Shrivastava, M. Warhadpande, R. Parekhji – Texas Instruments

2A.3 *Basing Acceptable Error-Tolerant Performance on Significance-Based Error-Rate (SBER) Devices,* Z. Pan, M. Breuer –Univ. of South. Cal.

1:20 pm – 2:20 pm

Aragon II Session 2B: **TEST AND DIAGNOSIS OF SCAN CHAINS**
Moderator: Bruce Cory – Nvidia

2B.1 *Diagnosis of Scan Clock Failures,* N. Basturkmen, K. L. Lee, S. Venkataraman – Intel

2B.2 *An Efficient Scan Chain Diagnosis Method Using a New Symbolic Simulation,* S. Chun, Y. Kim, T. Kim, S. Kang – Yonsei Univ.

2B.3 *On the Detectability of Scan Chain Internal Faults – An Industrial Case Study,* F. Yang – Univ. of Iowa, S. Chakravarty, N. Devta-Prasanna – LSI Logic, S. Reddy – Univ. of Iowa, Irith Pomeranz – Purdue Univ.

1:20 pm – 2:20 pm

Aragon III Session 2C: **DEVICE DEGRADATION AND INFANT MORTALITY**
Organizers: J. W. Tschanz – Intel
Moderator: G. Eide – Magma

2C.1 *Realistic Projections of Product Fmax and Vmin Shifts due to HCI, NBTI, and TDDB,* A. Haggag – Freescale

2C.2 *Comprehending NBTI at the Product Level,* V. Reddy – Texas Instruments

2C.3 *In-line Manufacturing Measurement of Infant Mortality Thermal Activation Energy,* A. Vassighi – Intel

2:20 pm – 2:40 pm BREAK

2:40 pm – 3:40 pm

Aragon I Session 3A: **MEMORY DIAGNOSIS AND REPAIR**
Moderator: M. Rodgers

3A.1 *An SRAM Design-for-Diagnosis Solution Based on Write Driver Voltage Sensing,* A. Ney, P. Girard, S. Pravossoudovitch, A. Virazel – LIRMM, M. Bastian, V. Gouin – Infineon

3A.2 *An Efficient March-Based Three-Phase Fault Location and Full Diagnosis Algorithm for Realistic Two-operation Dynamic Faults in Random Access Memories,* G. Harutyunyan, V. Vardanian – Virage Logic

3A.3 *Design and Analysis of a Self-Repairing SRAM with On-Chip Monitor and Compensation Circuitry,* N. Mojumder – Purdue Univ., S. Mukhopadhyay – Georgia Inst. of Tech., J. J. Kim, C.T. Chuang – IBM T. J. Watson Research Center, K. Roy – Purdue Univ.

2:40 pm – 3:40 pm

Aragon II Session 3B – SPECIAL SESSION
NEW TOPIC:
WHY NANOSCALE PHYSICS FAVORS QUANTUM INFORMATION &
WHY COMPUTING IS POSSIBLE IN SPITE OF QUANTUM UNCERTAINTY
Organizer: B. Courtois – TIMA
Moderator: B. Kaminska – Simon Fraser Univ.
Presenters:
I. Markov – Univ. of Michigan
J. Hayes – Univ. of Michigan

2:40 pm – 3:40 pm

Aragon III Session 3C: **AUTOMATIC TEST DEVELOPMENT FOR MIXED-SIGNAL/RF CIRCUITS**
Organizer: V. Zivkovic – NXP
Moderator: K. Arabi – Qualcomm

3C.1 *ATPG for SerDes Testing on any ATE, Bench-Top, or Simulator,* S. Sunter, A. Roy, G. Danialy – LogicVision

3C.2 *Test Verification and Program Generation for Modular System-on-Chips with Mixed Signal Cores,* V. Zivkovic, R. Jonker – NXP

3C.3 *Automating Test Development for Mixed-Signal and RF circuits -- Can Current Test Help?,* H. Manhaeve – Q-Star

3:40 pm – 4:00 pm BREAK

4:00 pm – 5:00 pm

Aragon I Session 4A: **MODELING AND TESTING FOR NANOMETER CMOS**
Moderator: S. Venkataraman – Intel

4A.1 *Gate Oxide Early Life Failure Prediction,* T. W. Chen, K. Kim, Y. M. Kim, S. Mitra – Stanford Univ.

4A.2 *Full Open Defects Under Tunneling Leakage Current in Nanometric CMOS,* D. A. Delgado, R. Rodriguez-Montanes, J. Figueras – Universitat Politècnica de Catalunya, S. Eichenberger, C. Hora, B. Kruseman – NXP

4A.3 *Signature Rollback – A Technique for Testing Robust Circuits,* U. Amgalan, C. Hachmann, S. Hellebrand – Univ. of Paderborn, H. J. Wunderlich - Univ. of Stuttgart

26th IEEE VLSI TEST SYMPOSIUM TECHNICAL PROGRAM
Monday, April 28th, 2008

4:00 pm – 5:00 pm

Aragon II Session 4B: **LOW POWER SCAN TESTING**
Moderator: C. Landrault – LIRMM

4B.1 *Bounded Adjacent Fill for Low Capture Power Scan Testing,* A. Chandra, R. Kapur – Synopsys

4B.2 *Reducing Scan Shift Power at RTL,* E. Alpaslan, J. Dworak – Brown Univ., Y. Huang, X. Lin, W. T. Cheng – Mentor Graphics

4B.3 *Scan-Chain Reordering for Minimizing Scan-Shift Power Based on Non-Specified Test Cubes,* J. Wu – National Chiao Tung Univ.

4:00 pm – 5:00 pm

Aragon III Session 4C: **BRIDGING PRE-SILICON VERIFICATION AND POST-SILICON VALIDATION AND DEBUG**
Organizers: E.J. Marinissen – NXP
Moderator: N. Nicolici – McMaster Univ.

4C.1 *Pre-Silicon Verification Perspective,* G. Shurek, A. Adir– IBM

4C.2 *Post-Silicon Design-for-Debug Perspective,* M. Abramovici, P. Bradley – DAFCA

4C.3 *Post-Silicon Hardware/Software Co-Debug Perspective,* B. Vermeulen, K. Goossens – NXP

8:00 pm – 9:30 pm

Aragon I Session 5A – SPECIAL SESSION
EMBEDDED TUTORIAL:
ROBUST DESIGN: TECHNIQUES AND TRENDS
Organizer: M. Zhang – Intel
Moderator: Z. Navabi – Worcester Poly
Presenters:
K. Roy – Purdue Univ. K. Agarwal – IBM
M. Zhang – Intel

8:00 pm – 9:30 pm

Aragon II Session 5B – SPECIAL SESSION
APPRENTICE – VTS EDITION
Organizer/Moderator: K. S. Kim – Intel
Presenters:
A. Crouch – Verigy J. Dastidar – Altera
A. Gattiker – IBM R. Kapur – Synopsys
S. Ozev – Duke Univ.

8:00 pm – 9:30 pm

Aragon III Session 5C – SPECIAL SESSION
Student Posters
Organizer: J. Plusquellic – UMBC

 - *Innovative Practices Session*

26th IEEE VLSI TEST SYMPOSIUM TECHNICAL PROGRAM Tuesday, April 29th, 2008

7:30 am – 8:30 am Registration, Coffee Service

8:30 am – 9:30 am

Aragon I Session 6A: **TESTING OF ANALOG CIRCUITS**
Moderator: J. M. Cooper – Intel

6A.1 *A Time-Domain Method for Pseudo-Spectral Characterization,* A. Mishra, M. Soma – Univ. of Washington

6A.2 *A Built-In TFT Array Charge-Sensing Technique for System-on-Panel Displays,* C. W. Lin, J. L. Huang – National Taiwan Univ.

6A.3 *Fast Accurate Tests for Multi-Carrier Transceiver Specifications: Phase Noise and EVM,* R. Senguttuvan, A. Chatterjee, S. Bhattacharya – Georgia Inst. of Tech.

8:30 am – 9:30 am

Aragon II Session 6B: **ATPG** I
Moderator: L. Miclea – U Tech of Cluj

6B.1 *Automatic Test Pattern Generation for Interconnect Open Defects,* S. Spinner, I. Polian, P. Engelke, B. Becker – Albert Ludwigs Univ. of Freiburg, M. Keim, W. T. Cheng – Mentor Graphics

6B.2 *On the Relaxation of N-detect Test Sets,* S. N. Neophytou, M. Michael – Univ. of Cyprus

6B.3 *Test-Pattern Ordering for Wafer-Level Test-During-Burn-In,* S. Bahukudumbi, K. Chakrabarty – Duke Univ.

8:30 am – 9:30 am

Aragon III Session 6C: **POST-SILICON VALIDATION: CURRENT PRACTICES AND NEW CHALLENGES**
Organizer: S. Gupta – Univ. of South. Cal.
Moderator: M. Hunt – Qualcomm

6C.1 *Post-Silicon Validation Challenges of Highly Integrated Processors,* P. Patra, C. Prudvi – Intel

6C.2 *A Bug's Life... and How the Test Research Community Can Shorten it,* I. Parulkar – Sun Microsystems

6C.3 *Optimizing ATPG Scan Stimulus for Post-Silicon Validation Debug with Diagnostic Equipment,* J. West, J. Drummond, C. Bullock, C. Pilch – Texas Instruments

9:30 am – 9:50 am BREAK

- *Innovative Practices Session*

26th IEEE VLSI TEST SYMPOSIUM TECHNICAL PROGRAM Tuesday, April 29th, 2008

9:50 am – 10:50 am

Aragon I Session 7A: **TESTING OF RF CIRCUITS**
Moderator: M. Sawan – Ecole Poly de Montreal

7A.1 *Low Cost RF Receiver Parameter Measurement with On-chip Amplitude Detectors,* C. Zhang, R. Gharpurey, J. Abraham – Univ. of Texas at Austin

7A.2 *An Integrated BiST Solution for Characterizing RF Transceivers Through a Single Measurement Tolerance,* E. Erdogan, S. Ozev – Duke Univ.

7A.3 *ACT: Adaptive Calibration Test Based Performance Improvement and Test Enhancement of Wireless RF Front Ends,* V. Natarajan, R. Senguttuvan, S. Sen, A. Chatterjee – Georgia Inst. of Tech.

9:50 am – 10:50 am

Aragon II Session 7B: **TESTING OF TRANSITION FAULTS AND SMALL DELAY DEFECTS**
Moderator: N. Touba – Univ. of Texas at Austin

7B.1 *Synthesis for Broadside Testability of Transition Faults,* I. Pomeranz – Purdue Univ, S. Reddy – Univ. of Iowa

7B.2 *LSTDF: Low-Switching Transition Delay Fault Pattern Generation,* M. Tehranipoor, J. Lee – Univ. of Connecticut

7B.3 *Test-Pattern Grading and Pattern Selection for Small-Delay Defects,* M. Yilmaz, K. Chakrabarty, – Duke Univ., M. Tehranipoor – Univ. of Connecticut

9:50 am – 10:50 am

Aragon III Session 7C: **DESIGN FOR YIELD AND MANUFACTURABILITY**
Organizer: S. Shoukourian – Virage Logic
Moderator: S. Taneja – Cadence

7C.1 *Performance Binning in the Presence of Process Variability,* A. Majumdar, V. Ganti - AMD

7C.2 *Yield Acceleration based on Design for Yield and Manufacturability,* Y. Zorian - Virage Logic

7C.3 *A Realistic View of DFM or Search for the Holy Grail,* Manuel d'Abreu - SanDisk

10:50 am – 11:10 am BREAK

■ - *Innovative Practices Session*

26th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Tuesday, April 29th, 2008

11:10 am – 12:10 pm

Aragon I Session 8A: **DELAY TEST AND MEASUREMENT**
Moderator: V. Agrawal – Auburn Univ.

8A.1 *Dynamic Compaction for High Quality Delay Test,* Z. Wang, D. Walker – Texas A&M Univ.

8A.2 *An All-Digital High-Precision Built-In Delay Time Measurement Circuit,* M. C. Tsai, C. H. Cheng – Feng-Chia Univ.

8A.3 *Error Sequence Analysis,* J. Lee, I. Park – Stanford Univ., E. McCluskey - Stanford CRC

11:10 am – 12:10 pm

Aragon II Session 8B: **TESTING AND ERROR TOLERANCE FOR EMERGENT TECHNOLOGY CIRCUITS**
Moderator: R. Makki – UAE Univ.

8B.1 *QBIST: 1-Testable Quantum Built-In Self-Test for any Boolean Circuit,* Y. H. Chou, I-M. Tsai, S. Y. Kuo – National Taiwan Univ.

8B.2 *A Statistical Approach to Characterizing and Testing Functionalized Nanowires,* J. Dardig, E. Stern, M. Reed, Y. Makris – Yale Univ., H. Stratigopoulos – TIMA

8B.3 *A Metric for Assessing the Error Tolerance of Tile Sets for Punctured DNA Self-assemblies,* M. Hashempour, Z. M. Arani, F. Lombardi – Northeastern Univ.

11:10 am – 12:10 pm

Aragon III Session 8C: **STIL UTILIZATION IN PRACTICE**
Organizer: K. Hatayama – STARC
Moderator: P. Mantri – Sun Microsystems

8C.1 *Building Standard Test Environment based on STIL,* H. Kamitokusari, T. Aikyo - STARC

8C.2 *A STIL-based Desktop ATPG Diagnostic Environment,* G.Danialy, S.Pateras– LogicVision

8C.3 *STILAccess: Shared Libraries for STIL Parser Modes,* H. Date – System JD

12:10 pm – 1:45 pm LUNCH

1:45 pm – 3:15 pm

Aragon I Session 9A – HOT TOPIC SESSION
YIELD MANAGEMENT & DPPM REDUCTION
Organizers:
P. Ehlig – Texas Instruments
A. Kokrady – Texas Instruments
Moderator: T. M. Mak – Intel

- *Innovative Practices Session*

9A.1 *Memory Yield Improvement through Multiple Test Sequences and Application-aware Fault Models,* A. Kokrady, C.P. Ravikumar, N. Chandrachoodan – Texas Instruments

9A.2 *Lithography and Memories: From Shapes to Electrical,* P. Gupta – Univ. of Cal. Los Angeles, C. Wu – Aprio Technologies

9A.3 *Panel Discussion: Yield Management and DPPM Reduction for Sub Micron Memories*
Presenters:
P. Ehlig – Texas Instruments
Y. Zorian – Virage Logic
R. Aitken – ARM

1:45 pm – 3:15 pm

Aragon II Session 9B – SPECIAL SESSION
EMBEDDED TUTORIAL: NANOELECTRONICS – WHAT NEXT? FROM MOORE'S LAW TO FEYNMAN'S VISION
Organizers:
S. Mourad – Santa Clara Univ.
Y. Zorian – Virage Logic
Moderator: S. Mourad – Santa Clara Univ.

9B.1 *One Dimensional Nanostructures and their Applications,* M. Meyyappan – NASA Ames Research Center

9B.2 *Emerging Nanoelectronic Devices,* B. Yu – UARC/NASA Ames Research Center

9B.3 *Carbon Nanostructures as On-chip Interconnects,* C. Y. Yang - Santa Clara Univ.

1:45 pm – 3:15 pm

Aragon III Session 9C – HOT TOPIC SESSION
TTTC 2008 BEST DOCTORAL THESIS CONTEST
Organizer: Y. Makris – Yale University
Moderator: H. Stratigopoulos – TIMA
Judges:
M. Abadir – Freescale
T. M. Mak – Intel
T. McLaurin – ARM
J. Rajski – Mentor Graphic
J. Saxena – Texas Instruments

3:30 pm – 11:00 pm

SOCIAL PROGRAM
See page 22 for more information.

26th IEEE VLSI TEST SYMPOSIUM TECHNICAL PROGRAM Wednesday, April 30th, 2008

8:00 am – 9:00 am Registration, Coffee Service

9:00 am – 10:00 am

Aragon I Session 10A: **TESTING OF MIXED SIGNAL CIRCUITS**
Moderator: I. Hartanto – Xilinx

10A.1 *Efficient Loopback Test for Aperture Jitter in Embedded Mixed-Signal Circuits,* B. Kim, J. Abraham – Univ. of Texas at Austin, N. Khouzam – National Semiconductor

10A.2 *Test Compaction for Mixed-Signal Circuits Using Pass-Fail Test Data,* S. Biswas, R. S. Blanton – Carnegie Mellon Univ.

10A.3 *Parallel Loopback Test of Mixed-Signal Circuits,* J. Park, H. Shin, J. Abraham – Univ. of Texas at Austin

9:00 am – 10:00 am

Aragon II Session 10B: **ATPG II**
Moderator: H. Konuk – Broadcom

10B.1 *Expanded Definition of Functional Operation Conditions and its Effects on the Computation of Functional Broadside Tests,* I. Pomeranz – Purdue Univ., S. Reddy – Univ. of Iowa

10B.2 *An ATPG Methodology to Detect Weight Related Defects in Threshold Logic Gates,* M. K. Goparaju, S. Tragoudas – Southern Illinois Univ.

10B.3 *Fault Nodes in Implication Graph for Equivalence/Dominance Collapsing, and Identifying Untestable and Independent Faults,* S. Rajamani – Qualcomm, M. Bushnell – Rutgers Univ., V. Agrawal – Auburn Univ.

9:00 am – 10:00 am

Aragon III Session 10C: **TESTING FOR COMPLEX FAILURE MECHANISMS AND PROCESS VARIATIONS OF MEMORIES**
Organizers: M. Azimane – NXP
Moderator: B. Wang – AMD

10C.1 *Dealing with Complex Failure Mechanisms for High Quality Testing in Embedded SRAMs,* M. Azimane, B.Kruseman, S. Eichenberger – NXP

10C.2 *Impact of Technology Scaling on Defects and Parameter Derivations in Embedded SRAMs,* L. Dilillo, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel – LIRMM, M. Bastian,V. Gouin – Infineon

- *Innovative Practices Session*

10C.3 *Flexible Memory Test Architectures for Combating Subtle Defects and Process Variations,* V. Jayaram, S. Lai – Texas Instruments

10:00 am – 10:20 am BREAK

10:20 am – 11:20 am

Aragon I Session 11A: **DEBUG AND DIAGNOSIS**
Moderator: M. Michael – Univ. of Cyprus

11A.1 *Fast Measurement of the "Non-deterministic Zone" in Microprocessor Debug using Maximum Likelihood Estimation,*
D. Tadesse, R. I. Bahar – Brown Univ., J. Grodstein – Intel

11A.2 *Expanding Trace Buffer Observation Window for In-System Silicon Debug through Selective Capture,* J. S. Yang, N. Touba – Univ. of Texas at Austin

11A.3 *A General Failure Candidate Ranking Framework,* C.C. Yen, S.T. Lin, H. Lin – Springsoft, K. Yang, Y. C. Hsu, T. Liu – Novas

10:20 am – 11:20 am

Aragon II Session 11B – SPECIAL SESSION
EMBEDDED TUTORIAL:
A SURVEY OF ON-CHIP DELAY MEASUREMENT TECHNIQUES FOR PRODUCTION TEST – FROM NANO TO PICOSECONDS
Organizer & Presenter: S. Sunter – LogicVision

10:20 am – 11:20 am

Aragon III Session 11C: **NEW EMERGING PRACTICES FOR SEMICONDUCTOR TEST**
Organizers: P. Roddy – Advantest
Moderator: D. Appello – ST Microelectronics

11C.1 *Development of Common Tools & Tester Language for ATE,* P. Decher – TSSI

11C.2 *New RF Testing Innovations,* K. Schaub – Advantest

11C.3 *Migration of PXI Instruments into Semiconductor Production Test,* E. Starkloff – National Instruments

11:20 am – 11:40 am BREAK

11:40 am – 12:40 pm

Aragon I Session 12A: **FAULT TOLERANCE**
Moderator: F. Lombardi – Northeastern Univ.

 - *Innovative Practices Session*

12A.1 *Algorithm Level Fault Tolerance: a New Technique to Cope with Radiation Induced Faults in Matrix Multiplication Algorithms,* C. Lisboa, L. Carro – Universidade Federal do Rio Grande do Sul, C. Argyrides, D. Pradhan – Bristol Univ.

12A.2 *Codeword Selection for Crosstalk Avoidance and Error Correction on Interconnects,* Y. Zhang, H. Li, X. Li, Y. Hu – Chinese Academy of Sciences

12A.3 *Low Cost Highly Robust Hardened Storage Cells Using Blocking Feedback Transistors,* M. Nicolaidis – TIMA, D. Alexandrescu, R. Perez – IRoC

11:40 am – 12:40 pm

Aragon II Session 12B: **TESTING OF PATH DELAY FAULTS**
Moderator: C. Aktouf – Defacto

12B.1 *Multiple Coupling Effects Oriented Path Delay Test Generation,* M. Zhang, H. Li, X. Li – Chinese Academy of Sciences

12B.2 *A Novel SBST Generation Technique for Path-Delay Faults in Microprocessors Based on BDD Analysis and Evolutionary Algorithm,* M. Grosso, P. Bernardi, E. Sanchez, M. Sonza Reorda – Politecnico di Torino, K. Christou, M. Michael – Univ. of Cyprus

12B.3 *An Industrial Case Study of Sticky Path-Delay Faults,* I. Huang, S. Gupta – Univ. of South. Cal., Y. S. Chang – Intel, S. Chakravarty – LSI Logic

11:40 am – 12:40 pm

Aragon III Session 12C: **FAULT LOCALIZATION PRACTICES AND CHALLENGES**
Organizer: S. Tammali – Texas Instruments
Moderator: B. Eklow – Cisco

12C.1 *Current practices of FA Engineer / DFT engineer and Challenges,* S. Tammali, K. Scott Wills, D. Paul – Texas Instruments

12C.2 *Principle and Practice of Modern Scan Diagnostics,* S. Cook, B. Benware – Mentor Graphics

12C.3 *Tester-based Scanning Optical Microscope Techniques for Fault Localization,* J. C. Phang – SEMICAPS, M. R. Bruce – AMD

12:40 pm – 2:00 pm LUNCH

- *Innovative Practices Session*

26th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Wednesday, April 30th, 2008

2:00 pm – 3:30 pm

Aragon I Session 13A – SPECIAL SESSION
PANEL:
MITIGATING RELIABILITY, YIELD AND POWER ISSUES IN NANO-CMOS: DESIGN PROBLEM OR EDA PROBLEM?
Organizer: M. Nicolaidis – TIMA
Moderator: Y. Zorian – Virage Logic
Co-Organized with:

Panelists:
S. Bhabhu – Cadence
R. A. Parekhji – Texas Instruments
M. Nicolaidis – TIMA
M. Zhang – Intel

2:00 pm – 3:30 pm

Aragon II Session 13B – HOT TOPIC SESSION
BIOMEDICAL DEVICES – NEW TEST CHALLENGES
Organizer: B. Kaminska – Simon Fraser Univ.
Moderator: K. Eshraghian– Univ. of Cal., Merced

13B.1 *Massively Parallel Wireless Sensing from the Cortex: Design and Test Challenges,* M. Sawan – Ecole Polytechnique

13B.2 *Design and Calibration of EEG Electrode Arrays for Wearable BCI,* G. Cauwenberghs – Univ. of Cal., San Diego

13B.3 *Testing of Digital Microfluidic Biochips: Fault Models, Test and Fault Diagnosis* K. Chakrabarty – Duke Univ.

2:00 pm – 3:30 pm

Aragon III Session 13C – SPECIAL SESSION
PANEL:
IS UBIQUITOUS RF AT ODDS WITH TEST?
Organizers: A. Khoche – Verigy
Moderator: A. Chatterjee – Georgia Inst. of Tech.
Panelists:
O. Martinez – Qualcomm
G. McCarter – Verigy
K. Harvey – Teradyne
K. Schaub – Advantest
P. Berndt – Cypress Semiconductor
M. Berry - Amkor

SOCIAL PROGRAM
Tuesday, April 29th, 2008

The Social Program will provide a relaxing atmosphere for networking and socializing, as well as an evening of entertainment.

For this year's social event we will journey south of the US border to visit Baja California, Mexico. The Tourist Corridor just south of the California border includes Tijuana, Ensenada and Rosarito. The region has long endeared itself to visiting Americans and International travelers in search of sprawling coastlines with a Southern California climate.

Our first stop will be Tecate, Mexico. Tecate offers a charming small-town ambience even today, an attraction that keeps bringing tourists into the town. There's a thriving artists' colony that influences the temper of the town. Rather than the usual curios found in border towns, local pottery, tile and glassworks are displayed at shops and handicraft centers, and local art is displayed at galleries around town. We will have time to sample local sweet breads and beer for which the town is famous, and visit Hidalgo Plaza, where visitors can enjoy Tecate's unique beauty.

Next, we visit Rosarito, Mexico. Rosarito lies along the sea coast, and has a mild climate with plenty of sun and a soft sea breeze. Each year, thousands of tourists run from the hustle and bustle of large cities to relax on the beaches of Rosarito.

We will dine at a beautiful beach-side resort in nearby Puerto Nuevo. We will be met with a welcome drink and enjoy the sunset and a nice dinner with traditional Mexican food and folkloric dance and mariachi.

Please do not forget to bring your passport to participate in this exciting excursion. Foreign visitors should ensure that they have double or multiple-entry visas to the US if necessary.

Busses will leave the Rancho Bernardo Inn at 3:30 p.m. and depart Baja at approximately 11 p.m. There is no extra cost for this program for VTS attendees who register at member and non-member rates. Students and companions of VTS attendees can register for the Social Program for $100 per person. To guarantee your participation in this program you must register before April 11, 2008.

TEST TECHNOLOGY EDUCATIONAL PROGRAM 2008

The Tutorials and Education Group of TTTC continues for a 9th year the organization of a comprehensive set of test technology tutorials. These comprise tutorials in conjunction with TTTC sponsored technical meetings, web-based tutorials, and on-site tutorials and courses. The tutorials are part of the successful annual Test Technology Educational Program (TTEP 2008).

TTEP intends to serve both test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics and also the opportunity to earn official certification from IEEE TTTC. Each six-hour tutorial corresponds to four TTEP units. Upon completion of each sixteen TTEP units official accreditation in the form of an "IEEE TTTC Test Technology Certificate" is presented to the participants.

The Test Technology Educational Program 2008 includes (but is not limited to) tutorial units presented in conjunction with the following TTTC sponsored technical meetings (in chronological order):

- Latin American Test Workshop (LATW'08), February 17–20, Puebla, Mexico
- Design Automation & Test in Europe Conference (DATE'08), March 10–14, Munich, Germany
- VLSI Test Symposium (VTS'08), April 27–May 1 , San Diego, California, USA
- Signal Propagation on Interconnects Workshop (SPI'08), May 12–15, Avignon, France
- International Conference on Automation, Quality&Testing, Robotics (AQTR'08), May 22-25, Cluj-Napoca, Romania
- European Test Symposium (ETS'08), May 25–29, Lago Maggiore, Italy
- International On-Line Testing Symposium (IOLTS'08), July 6–9, Rhodes, Greece
- International Test Conference (ITC'08), October 26–30, Santa Clara, California, USA
- Asian Test Symposium (ATS'08), November 24–27, Sapporo, Japan

INFORMATION: For further details about TTEP, please contact Tutorials and Education Group Chair Dimitris Gizopoulos (*dgizop@unipi.gr).* For a detailed list of tutorials and tutorial descriptions,

Please visit our web-site:

http://tab.computer.org/tttc/teg/ttep

Sunday, April 27th, 2008
TUTORIALS

VLSI Test Symposium 2008 includes three excellent TTEP 2008 tutorials on high interest test technology topics. All three tutorials qualify for IEEE TTTC certification. One tutorial will be presented on Sunday, April 27th and two on Thursday, May 1st. Each tutorial requires a separate fee and registration (see General Information, page 6).

7:30 am – 8:30 am Tutorial Registration, Coffee Service

8:30 am – 4:30 pm

Aragon IB

TUTORIAL 1: **SOFT ERRORS: TECHNOLOGY TRENDS, SYSTEM EFFECTS, PROTECTION TECHNIQUES AND CASE STUDIES**

Presenters:

Subhasish Mitra – Stanford University
Pia Sanda – IBM
Norbert Seifert – Intel

AUDIENCE: Researchers and practitioners interested in architecture, modeling, design, CAD, test and reliability.

DESCRIPTION: Radiation-induced soft errors are getting worse in digital systems manufactured in advanced technologies. Stringent data integrity and availability requirements of enterprise computing and networking applications demand special attention to soft errors in sequential elements and combinational logic. This tutorial discusses the impact of technology scaling on soft error rates, circuit-level modeling of soft errors, architectural impact of soft errors, challenges associated with evaluation of run-time behaviors of systems in the presence of soft errors, actual data on system behaviors in the presence of soft errors, metrics for quantifying soft error vulnerabilities, design of architectures with Built-in-Soft-Error-Resilience techniques, and actual case studies.

Thursday, May 1st, 2008
TUTORIALS

7:30 am – 8:30 am Tutorial Registration, Coffee Service

8:30 am – 4:30 pm
Aragon IIIA

TUTORIAL 2**: PRACTICES IN ANALOG, MIXED-SIGNAL AND RF TESTING**

Presenters:
Salem Abdennadher – Intel
Saghir Shaikh – Cadence

AUDIENCE: This tutorial is most suitable for design, test and DFT engineers involved in actual implementation of mixed-signal, analog, RF and wireless devices and systems. The architects and engineering managers would also greatly benefit from this tutorial.

DESCRIPTION: The objective of this tutorial is to present existing industry ATE solutions and alternatives to testing of mixed-signal and RF SoCs. These techniques greatly rely upon DFT and BIST structures. The tutorial presents the basic concepts in analog and RF measurements (eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, etc.). Several industrial examples of production testing of mixed-signal and RF devices, such as, SERDES transceivers, PHYs, HSIO, and RF transceivers are also presented. The block-DFT solutions are presented for PLLs, CDR, equalizers, filters, mixers, AGC, LNAs, DACs and ADCs. The testing of high speed IO interfaces, such as, PCIe, and SATA, etc, and the new design trends in RF systems such as MIMO and SiP based systems and their testability are also presented in this tutorial.

8:30 am – 4:30 pm
Aragon IIIB

TUTORIAL 3: **Statistical SCREENING METHODS Targeting "Zero Defect" IC Quality and Reliability**

Presenter:
Adit Singh – Auburn University

AUDIENCE: Test and Reliability Engineers, Engineering Managers, Reliability and Quality Assurance Managers, Researchers and Research Students.

DESCRIPTION: Integrated circuits have traditionally all been tested identically in the manufacturing flow. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by adaptively subjecting "suspect" parts to more extensive testing. The idea is similar to security screening at airports. Such methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production circuits from several companies.

IEEE Workshop on Test of Wireless Circuits and Systems

WTW 2008

April 27th, 2008

SCOPE: The Wireless Test Workshop (WTW) includes, among others, the following major topics in RF test: Case Studies, High-Frequency Test, Embedded RF Circuit Test, RF Test Board Related Issues, Yield Learning, Wireless Test Methodology, Standards Conformance Test, Noise Characterization and Validation, Economics of Test, Wireless Product Test Equipment and Metrology, Wafer Probing. For this year, the program committee has put together a highly technical program that includes: an invited speaker, 1 mini-tutorial, plus 10 other technical papers. The workshop encourages discussion and the technical program is oriented to create an atmosphere that facilitates audience learning and contribution to the subject matter.

Advance Program Summary:

1) Invited Speaker: “The Convergence of Media and Telecommunications Pushing Ahead”, Christopher Douglass, Wireless Strategy and Next Gen Solution Executive, IBM Global Telecommunications

2) Session #1: Next Generation Solutions

3) Session #2: Wafer Test

4) Session #3: On-Board/On-Chip DFT

5) Session #4: Reliability and RF DFT

REGISTRATION: All WTW 2008 participants require registration, which includes workshop technical sessions, workshop informal proceedings, break refreshments, and lunch.

SPONSORSHIP: WTW 2008 is sponsored by the IEEE Computer Society TTTC.

INFORMATION: For further details on the technical program, please contact Program Chair, Mustapha Slamani (*slamanim@us.ibm.com*). Regarding other questions, please contact the General Chair, Rob Aitken (*rob.aitken@arm.com*).

Please visit our web-site:

http://www.wtw2008.tec.ufl.edu/

IEEE International Workshop on Silicon Debug and Diagnosis

SDD 2008

April 30- May 1, 2008

Troubleshooting how and why systems and circuits fail is important to success in the modern electronic industries. Debug and diagnosis may be needed for yield improvement, process monitoring, correcting the design function, failure mode learning for R&D, or just getting a working first prototype. This detective work can however become very tricky. Sources of difficulty include circuit and system complexity, packaging, limited physical access, shortened product creation cycle and time-to-market, the traditional focus on only pass/fail testing and missing tool/equipment capabilities. Because of this new and efficient solutions for debug and diagnosis have a highly visible impact on productivity.

SDD 2008 is the fifth in a series of very successful discussion-oriented technical workshops. Its mission and objective is to consider all issues related to debug and diagnosis of systems and circuits - from design to prototype bring-up to volume production.

Advance Program Summary:

1) Keynote Speaker: Dr. Dipu Pramanik, VP R&D Design For Manufacturability Business Unit, Cadence

2) Four Technical Papers Sessions covering Debug Techniques and Methodologies, Debug and Test, Debug Standardization, and Industrial Case Studies.

3) Three Special Sessions presenting IEEE P1687 update, Innovative Debug Techniques, ATE's role in SDD.

Complete advanced program available at www.sdd-online.org

REGISTRATION: All SDD 2008 participants require registration, which includes workshop technical sessions, workshop informal proceedings, reception dinner on April 30th, continental breakfast, break refreshments, and lunch.

SPONSORSHIP: SDD 2008 is sponsored by the IEEE Computer Society TTTC.

INFORMATION: For further details on the technical program, please contact Program Chair, Bart Vermeulen (*bart.vermeulen@nxp.com*). Regarding other questions, please contact the General Chair, Fidel Muradali (*fidel.muradali@nsc.com*).

Please visit our web-site:

http://www.sdd-online.org/

IEEE
Design & Test of Computers

IEEE D&T is a bimonthly magazine published by the IEEE Computer Society iin cooperation with the IEEE Council on Electronic Design Automation and the IEEE Circuits and Systems Society specifically for design and test engineers, and researchers. D&T features peer-reviewed original work describing methods and practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

- System Level Design and Test
- Embedded Test Technology
- Low Power Design
- Reconfigurable Systems
- Board and System Test
- Analog and Mixed Signal Design and Test
- System-on-Chip Design and IP Reuse
- Embedded Systems and Software
- Design and Verification/Validation

In addition, D&T publishes tutorial articles, perspectives, roundtable discussions, book reviews, viewpoints, conference reports, panel summaries, and standards updates contributed by authors working in the industry.

PAPER SUBMISSION: Authors should use *Manuscript Central* (https://mc.manuscriptcentral.com/cs-ieee) to upload their submissions. The first-time user must create a new account. The site provides detailed instructions on usage. Each submitted paper undergoes at least three technical reviews. All submissions must be original, previously unpublished work.

SPECIAL ISSUES: The theme issues for 2008 are (please check D&T website for submission instructions and deadlines):

Jan/Feb	Design and Test of RFIC
March/April	The Current State of Test Compression
May/June	Silicon Debugging and Diagnosis
July/August	Design in the Late- and Post-Silicon Eras
Sep/Oct	Design and Test of Interconnects for Multi-Core Chips
Nov/Dec	IEEE Std 1500 and Its Usage

SUBSCRIPTION: IEEE D&T offers full year and half-year subscriptions for print issues. In addition, it offers to IEEE CS and CAS members electronic subscription options with full text searchable access to all issues from 1995 forward! A mirror image of the print issues, IEEE D&T's Digital Edition, is also available at qmags.com/dnt which is offered in a quick-downloading and searchable PDF format.

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26th IEEE VLSI Test Symposium (VTS 2008)

Sunday, April 27th, 2008

Time		
7:30 am – 8:30 am	TUTORIAL 1/ WORKSHOP (WTW08) REGISTRATION	
8:30 am – 4:30 pm	WORKSHOP: WTW 2008 *(8:30 am – 5:30 pm)*	Tutorial 1: Soft Errors: Technology Trends, System Effects, Protection Techniques and Case Studies

Monday, April 28th, 2008

Time			
7:30 am – 9:00 am	REGISTRATION		
9:00 am – 10:30 am	PLENARY SESSION		
11:00 am – 12:00 pm	Session 1A: Testing for High Speed Communication Systems	Session 1B: Compaction for Testing	Session 1C: Highways to Zero-Defects
1:20 pm – 2:20 pm	Session 2A: ATE Data Volume and False/Acceptable Test Fails	Session 2B: Test and Diagnosis of Scan Chains	Session 2C: Device Degradation and Infant Mortality
2:40 pm – 3:40 pm	Session 3A: Memory Diagnosis and Repair	Session 3B: New Topic: Why Nanoscale Physics Favors Quantum Information	Session 3C: Automatic Test Development for Mixed-Signal/RF Circuits
4:00 pm – 5:00 pm	Session 4A: Modeling and Testing for Nanometer CMOS	Session 4B: Low Power Scan Testing	Session 4C: Pre-Silicon Verification & Post-Silicon Validation/Debug
8:00 pm – 9:30 pm	Session 5A : Embedded Tutorial: Robust Design: Techniques and Trends	Session 5B: Apprentice – VTS Edition	Session 5C: Student Posters

Tuesday, April 29th, 2008

Time			
7:30 am - 8:30 am	REGISTRATION		
8:30 am – 9:30 am	Session 6A: Testing of Analog Circuits	Session 6B: ATPG I	Session 6C: Post-Silicon Validation
9:50 am - 10:50 am	Session 7A: Testing of RF Circuits	Session 7B: Testing of Transition Faults and Small Delay Defects	Session 7C: Design for Yield and Manufacturability

11:10 am – 12:10 pm	Session 8A: Delay Test and Measurement	Session 8B: Testing & Error Tolerance for Emergent Technology Circuits	Session 8C: STIL Utilization in Practice
1:45 pm – 3:15 pm	Session 9A: Hot Topic: Yield Management and DPPM Reduction	Session 9B: Embedded Tutorial: Nanoelectronics – What Next?	Session 9C: Hot Topic: TTTC 2008 Best Doctoral Thesis Contest
3:30 pm – 11:00 pm	Social Program		

Wednesday,April 30th, 2008

7:30 am - 9:00 am	REGISTRATION		
9:00 am – 10:00 am	Session 10A: Testing of Mixed Signal Circuits	Session 10B: ATPG II	Session 10C: Complex Failure & Process Variations of Memories
10:20 am – 11:20 am	Session 11A: Debug and Diagnosis	Session 11B: Embedded Tutorial: Survey of On-Chip Delay Measurement for Production Test	Session 11C: New Emerging Practices for Semiconductor Test
11:40 am – 12:40 pm	Session 12A: Fault Tolerance	Session 12B: Testing of Path Delay Faults	Session 12C: Fault Localization Practices and Challenges
2:00 pm – 3:30 pm	Session 13A: Panel: Reliability, Yield and Power Issues in Nano-CMOS	Session 13B: Hot Topic: Biomedical Devices -- New Test Challenges	Session 13C: Panel: Is Ubiquitous RF at Odds with Test?
4:00 pm - 6:00 pm	WORKSHOP: SDD 2008		

Thursday, May 1st, 2008

7:30 am – 8:30 am	TUTORIAL 2&3/WORKSHOP (SDD08) REGISTRATION	
8:30 am - 4:30 pm	Tutorial 2: Practices in Analog, Mixed-Signal and RF Testing	Tutorial 3: Statistical Screening Methods Targeting “Zero Defect” IC Quality and Reliability
8:00 am - 5:30 pm	WORKSHOP: SDD2008	

- *Innovative Practices Session*   - *Special Session*   - *VTS Lunch Break at Aragon Lawn*

26th IEEE VLSI Test Symposium (VTS 2008)
FRINGE TECHNICAL MEETINGS

A number of TTTC professional groups interested in test will hold their meetings at VTS 2008. At press time, the following meetings were scheduled. These meetings are for members. If you'd like to attend, please contact the person listed at the e-mail address given. Unless specified, all fringe meeting will be held in **Santa Catalina West** room.

MONDAY, April 28th

*12:00 pm - 1:20 pm	**Test Week Workshop Coordination** Yervant Zorian (*zorian@viragelogic.com*)
2:00 pm - 3:00 pm	**TTTC Tutorials and Education Group** Dimitris Gizopoulos (*dgizop@unipi.gr*)
3:00 pm - 4:00 pm	**TTTC Executive Committee** Adit Singh (*adsingh@eng.auburn.edu*)
4:00 pm - 5:00 pm	**ITRS Test Open Meeting** Mike Rodgers *(mjrodge2@sbcglobal.net)*
5:00 pm - 6:00 pm	**TTTC Senior Leadership Board** Yervant Zorian (*zorian@viragelogic.com*)
**6:00 pm - 8:00 pm	**IEEE VTS Program Committee** Peter Maxwell (*pmaxwell@micron*.com) Cecilia Metra (cmetra@deis.unibo.it)

TUESDAY, April 29th

8:00 am - 9:30 am	**TTTC Technical Meetings Review Committee** Chen-Huan Chiang (*chenhuan@alcatel-lucent.com*)
11:00 am - 12:00 pm	**ITRS DFT SubTeam** Yervant Zorian (*zorian@viragelogic.com*)
*12:10 pm - 1:45 pm	**TTTC Standards Group** Rohit Kapur *(rohit.kapur@synopsys.com)*
*12:10 pm - 1:45 pm	**Int'l OnLine Test Symposium Committee** Michael Nicolaidis *(michael.nicolaidis@imag.fr)*
2:00 pm - 3:00 pm	**TTTC Communications Group** Cecilia Metra (cmetra@deis.unibo.it)

WEDNESDAY, April 30th

8:00 am - 9:30 am	**TTTC Operations Committee** Adit Singh (*adsingh@eng.auburn.edu*)
10:00 am - 12:00 pm	**IEEE VTS Organizing Committee** Alex Orailoglu (*alex@cs.ucsd.edu*)
*12:10 pm - 1:45 pm	**TTTC Middle East and Africa Group** Rafic Makki (*makki@uaeu.ac.ae*)

**Meeting During Lunch Break*
***Meeting During Dinner at San Bernardo West*