26th IEEE VLSI TEST SYMPOSIUM (VTS2008)
Rancho Bernardo Inn, San Diego, California, USA
Apr 27th – May 1st, 2008
http://www.tttc-vts.org/

Call for Participation

The IEEE VLSI Test Symposium explores emerging trends and novel concepts in the testing of integrated circuits and systems. The symposium is a leading international forum where many of the world's leading test experts and professionals from both industry and academia join to present and debate key issues in testing. VTS 2008 addresses key trends and challenges in the semiconductor design and manufacturing industries through an exciting program that includes Keynote and Plenary Talks, Technical Paper Sessions, Embedded Tutorials, Panels, Hot Topic Sessions, Full-day Tutorials, co-located Workshops, and the Innovative Practices Track.

Plenary Session

Keynote Speaker
- Michael Campbell, Senior Vice President of Engineering, Qualcomm CDMA Technologies

Invited Keynote
- "A Revolution in Design and Test Technology," Prof. Melvin Breuer, University of Southern California

TECHNICAL PAPER SESSIONS will present the latest research results in test, including:

- Testing for High Speed Communication Systems
- Compaction for Testing
- ATE Data Volume
- Test & Diagnosis of Scan Chains
- Memory Diagnosis and Repair
- Testing for Nanometer CMOS
- Low Power Scan Testing
- Testing of Analog Circuits
- ATPG Techniques
- Testing of RF Circuits
- Transition Faults
- Delay Test and Path Delay Faults
- Testing and Error Tolerance for Emergent Technology Circuits
- Testing of Mixed Signal Circuits
- Debug and Diagnosis
- Fault Tolerance

INNOVATIVE PRACTICES (IP) TRACK highlights cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them.

- Highways to Zero-defects
- Device Degradation and Infant Mortality
- Automatic Test Development for Mixed-Signal/RF Circuits
- Pre-Silicon Verification & Post-Silicon Validation and Debug
- Design for Yield and Manufacturability
- STIL Utilization in Practice
- Testing for Complex Failures and Process Variations of Memories
- New Emerging Practices for Semiconductor Test
- Fault Localization Practices and Challenges

SPECIAL SESSIONS will include:

- EMBEDDED TUTORIALS: Robust Design, Nanoelectronics, Measuring IC Timing Parameters
- HOT TOPICS: Yield Management and DPPM Reduction, Biomedical Devices - New Test Challenges
- NEW TOPIC: Quantum Computing
- PANELS: Mitigating Reliability, Yield and Power Issues in Nano-CMOS: Design Problem or EDA Problem?; Is Ubiquitous RF at Odds with Test?; APPRENTICE: VTS Edition
- TTTC 2008 Best Doctoral Thesis Contest
- Student Posters

FULL-DAY WORKSHOPS and TUTORIALS complement the core technical program of VTS.

WORKSHOPS
- IEEE Workshop on Test of Wireless Circuits and Systems (WTW)
- IEEE International Workshop on Silicon Debug and Diagnosis (SDD)

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) TUTORIALS
- Soft Errors: Technology Trends, System Effects, Protection Techniques and Case Studies
- Practices in Analog, Mixed-signal and RF Testing

The social program at VTS provides an opportunity for informal technical discussions among participants. San Diego, California and Baja California, Mexico, provide very attractive backdrop for all VTS 2008 activities. We are sure that you will find VTS 2008 enlightening, thought-provoking, rewarding, and enjoyable!

VTS 2008 is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society. For more information on VTS 2008, visit the VTS website at http://www.tttc-vts.org or contact:

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