26th IEEE VLSI TEST SYMPOSIUM

Rancho Bernardo Inn, San Diego, California, USA

Apr 27th – May 1st, 2008

Call for Papers

The **IEEE VLSI Test Symposium** (VTS) explores emerging trends and novel concepts in test, diagnosis, and verification of electronic circuits and systems. Major topics include, but are not limited to:

- *Analog, M-S & RF Test*
- *Automatic Test Generation*
- *ATE Architecture & SW*
- *Board & System Test*
- *Built-In Self-Test (BIST)*
- *Current Based Test*
- *Defect Tolerance*
- *Delay & Performance Test*
- *Design for Testability (DFT)*
- *Design Verification/ Validation*
- *Diagnosis and Silicon Debug*
- *Embedded System Test*
- *Embedded Test Methods*
- *Fault Modeling and Simulation*
- *Infrastructure IP*
- *MEMS Test*
- *Memory Test and Repair*
- *Microprocessor Test*
- *Multi-Chip Module Test*
- *Nanometer Technologies Test*
- *On-Line Test*
- *Power Issues in Test*
- *Self-Repair & Fault Tolerance*
- *System-on-Chip (SOC) Test*
- *System-in-Package Test*
- *Test Resource Partitioning*
- *Thermal Test*
- *Test Data Compression*
- *Test of High-Speed I/O*
- *Test Quality and Reliability*
- *Test Resource Partitioning*
- *Transients and Soft Errors*
- *Yield Analysis & Optimization*

The VTS Program Committee invites **original, unpublished paper submissions** for VTS 2008**.** Paper submissions should be complete manuscripts, up to eight pages (inclusive of figures, tables, and bibliography) in a standard IEEE two-column format; papers exceeding the page limit will be returned without review. Authors should clearly explain the significance of the work, highlight novel features, and describe its current status. On the title page, please include: author name(s) and affiliation(s), and the mailing address, phone number, fax number, and e-mail address of the contact author. A 50-word abstract and five keywords identifying the topic area are also required.

Proposals for the **Innovative Practices track,** and **Special Sessions** are also invited**.** The innovative practices track will highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. Special sessions can include panels, embedded tutorials, or hot topic presentations. Innovative practices track and special session proposals should include a title, name and contact information of the session organizer(s), a 150-to-200 word abstract, and a list of prospective participants.

All submissions are to be made electronically through the VTS website. The deadline for submission of the abstract of a regular paper is **October, 29 2007**. (The submission of the full version of the regular paper is due a week later on **November 5, 2007.**) Detailed instructions for submissions are to be found at the conference website **http://www.tttc-vts.org.** Authors will be notified of the disposition of their papers by December, 21st 2007. A submission will be considered as evidence that, upon acceptance, the author(s) will present the paper at the symposium, and will submit a final camera-ready version of the paper for inclusion in the proceedings. In the case of innovative practice and special sessions, the organizers commit to submit a session title, abstract, and list of participants for inclusion in the symposium proceedings and program.

VTS 2008 will present a **Best Paper Award**, a **Best Panel Award**, and a **Best IP Track Session Award** based on the evaluations of reviewers, attendees, and an invited panel of judges.

TTTC Test Technology Educational Program (TTEP) tutorials on emerging test technology topics will be offered during VTS 2008. Tutorial proposals should be submitted according to TTEP 2008 submission deadlines (http://computer.org/tab/tttc/teg/ttep).

VTS 2008 is sponsored by the Test Technology Technical Council (TTTC) of the IEEE Computer Society. For more information on the VTS 2008, visit its website at *http://www.tttc-vts.org* or contact**:**

For general information:

GENERAL CHAIR
Alex Orailoglu
University of California, San Diego
Computer Science and Engineering
9500 Gilman Drive, Mail Code 0404
La Jolla, CA 92093-0404, USA
T: +1-858-534-0914
F: +1-858-534-7029
E: alex@cs.ucsd.edu

For submission related information:

PROGRAM CO-CHAIR
Peter Maxwell
Micron Technology
3080 North 1st Street, MS 65-300
San Jose, CA 95134, USA

T: +1 408 834 1643
F: +1 408 834 1223
E: pmaxwell@micron.com

PROGRAM CO-CHAIR
Cecilia Metra
ARCES - University of Bologna
Viale Risorgimento 2
40136 Bologna, Italy

T: + 39 051 209 3038
F: + 39 051 209 3073
E: cmetra@deis.unibo.it

IEEE VLSI Test Symposium
1474 Freeman Drive
Amissville, VA 20106, USA
Tel: +1-540-937-8280 Fax: +1-540-937-7848
Email: tttc@computer.org