Technical Program

25th IEEE

VLSI TEST SYMPOSIUM (VTS 2007)

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25th IEEE VLSI TEST SYMPOSIUM (VTS 2007)

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25th IEEE VLSI Test Symposium
VTS 2007
May 6-10, 2007
Claremont Resort
Berkeley, California, USA
INTRODUCTION

Welcome to VTS 2007, the twenty-fifth in a series of annual symposia that focus on innovation in the field of testing of integrated circuits and systems.

The core of VTS 2007, the three day technical program, responds to the many trends and challenges in the semiconductor design and manufacturing industries with papers covering a diverse and seminal set of topics including, RF and Analog Test, Delay Test, Memory Test, Diagnosis, Online Test, SoC Test, and Fault Prediction and Evaluation.

In addition to the three-day technical program, VTS 2007 features special sessions, and the Innovative Practices track. These tracks highlight cutting-edge challenges faced by test practitioners, and innovative solutions employed to address them. Full-day tutorials and workshops are also held in conjunction with VTS 2007. The Open Source Test Technology Tools Workshop continues its association with VTS. So does the Wireless Test Workshop which will be co-located with VTS this year for a second time. Three tutorials are offered by the TTTC Tutorials & Education Group through the Test Technology Education Program (TTEP). The tutorials by leading VLSI test academics and practitioners provide an introduction to a diverse set of topics, including Delay Test, Timing Issues, and the Interactions of Design and Test. The tutorials provide opportunities for design and test professionals to update their knowledge-base in test, and earn official IEEE TTTC accreditation.

The social program at VTS provides an opportunity for informal technical discussions among participants. Berkeley, California, provides a highly attractive backdrop for all VTS 2007 activities.

VTS is the result of the work of many dedicated volunteers: the reviewers, the best paper award judges, the Program Committee, the Organizing Committee, and the Steering Committee. We wholeheartedly thank them all. We also wish to thank all the authors who submitted their research to VTS 2007, and the program participants for their contribution at the symposium. We thank the IEEE Computer Society Test

INTRODUCTION (Continued)

Technology Technical Council for its continued sponsorship and support. And most importantly, we would like to offer a heartfelt word of thanks to all the Corporate Supporters of VTS 2007 who have contributed generously.

We hope that you will find VTS 2007 enlightening, thought-provoking, rewarding, and enjoyable. We wish you all a fun-filled and productive week in Berkeley and hope that you will keep making VTS a success by actively participating in it, assisting in its organization, and letting us always know when we can do something better. Thank you all for coming.

Paolo Prinetto
General Chair

Alex Orailoglu
Program Chair

The IEEE VLSI TEST SYMPOSIUM is sponsored by the IEEE COMPUTER SOCIETY'S Test Technology Technical Council (TTTC)

The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members' professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology.

TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters, and electronic broadcasts. All its activities are led by volunteer members.

TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. You may enroll as TTTC member for 2007 (no dues or fees) by using the embedded VTS 2007 Registration Form. To learn more about TTTC offerings and membership benefits, please visit:

http://tab.computer.org/tttc

25th IEEE VLSI TEST SYMPOSIUM
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25th IEEE VLSI TEST SYMPOSIUM GENERAL INFORMATION

All activities require a registration badge for admittance. All participants must pay the appropriate fees. Reduced fees are available to IEEE or Computer Society members on presentation of a valid member number.

To register, use the Symposium Registration Form. To receive early registration discount rates, your completed Registration Form must be RECEIVED in the VTS office by mail or fax by April 23, 2007. Until April 23, you may register online at:

www.tttc-vts.org

After April 23, advance registration will no longer be available and you must register at the hotel at the higher rates listed in the table. After April 23 SPACE IS NOT GUARANTEED in the Social Program.

Technical program registration includes a copy of the Proceedings, the social program, two luncheons, three continental breakfasts, and five coffee breaks. Student registration does not include the social program. Students and companions of registered attendees can buy tickets for the social program at $100 per person. Extra copies of the Proceedings are available at $50 each. Lunch tickets for companions of registered attendees will be available at the symposium ($35 each).

The Registration Form allows you to automatically enroll or renew your TTTC membership (no dues or fees) by checking the corresponding box.

The Wireless Test Workshop (WTW 2007) will take place May 6th from 8:30 am to 5:30 pm. Registration includes workshop technical sessions, workshop informal proceedings, break refreshments, and lunch.

The International Workshop on Open Source Test Technology Tools (IOST3 2007) will take place May 9th from 4:00 pm to 6:00 pm, and May 10th from 8:00 am to 5:30 pm. Registration includes workshop technical sessions, workshop informal proceedings, break refreshments, and lunch.

Tutorial registration for members and non-members includes lecturer's notes, breaks, and lunch.

REGISTRATION FEES:

Early Registration*	IEEE/CS Member	Student Member	Non-Member	Non-Member
SYMPOSIUM	$450	$140	$180	$570
TUT. 1	$320	$320	$400	$400
TUT. 2 or 3	$320	$320	$400	$400
WTW	$200	$115	$150	$275
IOST3	$200	$100	$125	$250

Registration At Hotel	IEEE/CS Member	Student Member	Non-Member	Non-Member
SYMPOSIUM	$540	$180	$225	$685
TUT. 1	$385	$385	$480	$480
TUT. 2 or 3	$385	$385	$480	$480
WTW	$275	$180	$225	$345
IOST3	$250	$150	$225	$360

*Social Program Fee** $100*

**discounts available through April 23, 2007*
***for students and companions of registered attendees*

REFUNDS: If you must cancel, advance registration fees will be refunded only upon written request to: VLSI Test Symposium, 1474 Freeman Drive, Amissville, VA, 20106, USA postmarked on or before April 23, 2007. A $50 processing fee is charged for each refund.

25th IEEE VLSI TEST SYMPOSIUM
TRAVEL INFORMATION

AIR

Two major airports serve the Berkeley, California area: San Francisco International Airport and Oakland International Airport.

AIRPORT GROUND TRANSPORTATION

SPECIAL CAR RENTAL DISCOUNTS!

We are pleased to announce that **Budget Rent a Car** is the official car rental car company of the 2007 VLSI Test Symposium.

- For special car rental discounts contact Budget Rent a Car at 1-800-772-3773 or you may make your reservations online at www.budget.com. Please use the Convention Discount Number **U063666**. This will ensure you receive the lowest rate possible.

Cab fare **from San Francisco International Airport** to The Claremont Resort & Spa costs approximately $47.00 one way. Cab fare **from Oakland International Airport** to The Claremont Resort & Spa costs approximately $37.00 one way.

SUPER SHUTTLE: To book online, go to www.supershuttle.com for airport transfers or call 1-800-BlueVan to ask about charters. Use Discount Code: **Q87QL**. This will ensure you receive all applicable discounts available.

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DIRECTIONS TO THE CLAREMONT RESORT & SPA

From San Francisco International Airport

- Follow signs for Hwy 101 North to San Francisco
- Take Hwy 80 East to the Bay Bridge to Oakland
- Cross Bay Bridge on Hwy 80, follow to 580 East
- Exit onto Hwy 24 to Berkeley/Walnut Creek
- Take the Claremont Avenue exit, turning left at the bottom of the exit onto Claremont
- Turn right on Ashby Avenue (5th stoplight)
- The Hotel's entrance is two blocks ahead on the left

From Oakland International Airport

- Go straight out of the airport on Airport Boulevard
- Turn right on Hegenberger Road
- From Hegenberger follow signs for 880 North
- From Hwy 880 North, follow signs for Hwy 24 to Walnut Creek
- Take the Claremont Avenue exit, turning left at the bottom of the exit onto Claremont
- Turn right on Ashby Avenue (5th stoplight)
- The Hotel's entrance is two blocks ahead on the left

25th IEEE VLSI TEST SYMPOSIUM
HOTEL INFORMATION

The 25th IEEE VLSI Test Symposium will be held at The Claremont Resort & Spa in Berkeley, California. Nestled in the beautiful hills facing one of the world's great travel destinations, the Claremont Resort & Spa opened in 1915 and gained a reputation as a retreat for wealthy San Franciscans to escape the fog on "the sunny side of the Bay." Majestically resting on 22 acres of beautifully landscaped gardens, its panoramic views of the Bay and city skyline are unequalled. Just twelve miles to downtown San Francisco and an hour's drive to California's renowned wine country, the Claremont's location makes it ideal for business or pleasure. Rich in history, the Claremont's warmth, character, and quintessential taste provides an experience which embraces the grace of the past with the strength of the future.

No daily resort fee will apply. Discounted parking will be provided for attendees at the rate of $12 per day. Parking tickets will be stamped at the VTS registration desk.

To contact the hotel:

The Claremont Resort & Spa
41 Tunnel Road
Berkeley, CA 94705
Tel: +1-800-551-7266 or +1-510-549-8595
www.claremontresort.com

To cancel a reservation and receive a refund, you must notify the resort at least 48 hours prior to your arrival date.

25th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Monday, May 7th, 2007

7:30 am – 9:00 am Registration, Continental Breakfast

9:00 am – 10:30 am

Empire Ballroom

PLENARY SESSION

Welcome Message:
Paolo Prinetto, VTS 2007 General Chair

Keynote Address:
"New Role of Test in 45 Nanometer,"
Antun Domic, Senior Vice President and General Manager, Implementation Group, Synopsys

Program Introduction:
Alex Orailoglu, VTS 2007 Program Chair

Invited Keynote:
"Roadmap of Design," Gary Smith, President Gary Smith EDA

25th Anniversary VLSI Test Symposium:
Yervant Zorian, 25th Anniversary VTS Chair

Awards Presentation:
TTTC Most Successful Technical Meeting Award
TTTC Most Populous Technical Meeting Award
VTS 2006 Best Paper Award
VTS 2006 Best Panel Award
VTS 2006 Best Innovative Practices Award

10:30 am – 11:00 am BREAK

11:00 am – 12:00 pm

Empire Ballroom

Session 1A: **RF TESTING I**
Moderator: B. Courtois – TIMA Labs

1A.1 *A Low-cost RF MIMO Test Method Using a Single Measurement Set-up,* E. Acar, S. Ozev – Duke Univ.; K.B. Redmond – Intel

1A.2 *Non-RF to RF Test Correlation Using Learning Machines: A Case Study,* H-G.D. Stratigopoulos – TIMA Labs; P. Drineas – RPI; M. Slamani – IBM; Y. Makris – Yale Univ.

1A.3 *RF Digital Signal Generation Beyond Nyquist,* M. Negreiros, L. Carro, A.A. Susin – UFRGS; A. Souza Jr. – CEFET-RS

11:00 am – 12:00 pm

Napa 1, 2, 3

Session 1B: **DELAY TEST QUALITY**
Moderator: P. Girard – LIRMM

1B.1 *Delay Test Quality Evaluation Using Bounded Gate Delays,* S. Bose – Intel; V. Agrawal – Auburn Univ.

1B.2 *On Performance Testing With Path Delay Patterns,* B. Kruseman, A. Majhi, G. Gronthoud – NXP Semiconductors

1B.3 *Power Virus Generation Using Behavioral Models of Circuits,* K. Najeeb; V.V.R. Konda, S.K.S. Hari, V. Kamakoti – IIT Madras; V.M. Vedula – Intel

11:00 am – 12:00 pm

Sonoma Session 1C: **DESIGN IN THE PRESENCE OF VARIATIONS: CHARACTERIZATION, MONITORING, AND RESPONSE**
Organizer: J.W. Tschanz – Intel
Moderator: S. Mourad - Santa Clara Univ.

1C.1 *Circuit-Based Process Variation Monitoring Techniques,* M. Craig – AMD

1C.2 *Test and Bringup Utilizing On-Chip Timing Monitors,* A. Drake – IBM

1C.3 *Dynamic Response to Temperature, Voltage, and Aging Variations,* J.W. Tschanz – Intel

12:00 pm – 1:20 pm LUNCH

1:20 pm – 2:20 pm

Empire Ballroom Session 2A: **MEMORY TEST**
Moderator: S. Al-Harbi – Kuwait Univ.

2A.1 *Retention and Reliability Problems in Embedded Flash Memories: Analysis and Test of Defective 2T-FLOTOX Tunnel Window,* O. Ginez, J.-M. Daga – Atmel; P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel – LIRMM

2A.2 *SDRAM Delay Fault Modeling and Performance Testing,* Y.-T. Hsing, C.-C. Huang, J.-C. Yeh, C.-W. Wu – Natl. Tsing Hua Univ.

2A.3 *Optimizing Test Length for Soft Faults in DRAM Devices,* Z. Al-Ars, S. Hamdioui, G. Gaydadjiev – Delft Univ. of Technology

1:20 pm – 2:20 pm

Napa 1, 2, 3 Session 2B: **TEST COMPRESSION**
Moderator: S. Hellebrand – Univ. of Paderborn

2B.1 *Minimizing the Impact of Scan Compression,* P. Wohl, J.A. Waicukauski, R. Kapur, S. Ramnath, E. Gizdarski, T.W. Williams, P. Jaini – Synopsys

2B.2 *Low Power Embedded Deterministic Test,* D. Czysz, J. Tyszer – Poznan Univ. of Technology; G. Mrugalski, J. Rajski – Mentor Graphics

2B.3 *Multimode Illinois Scan Architecture for Test Application Time and Test Data Volume Reduction,* A. Chandra, H. Yan, R. Kapur – Synopsys

1:20 pm – 2:20 pm

Sonoma Session 2C: **SMALL DELAY TEST IN PRACTICE**
Organizer/Moderator:
T. Jackson – Cadence

2C.1 *New Launch-off-Shift Technique to Improve At-Speed Test Quality,* M. Takakura, Y. Fukui, K. Tachikawa, Y. Maeda – Renesas

2C.2 *Testing for Small-Delay Defects at Azul,* S. Maker, T. Altinis, J. Wu, N. Patkar – Azul Systems

2C.3 *The Changing Role of Delay Testing Due to Variability & Systematic Failure Modes,* P. Nigh – IBM

2:20 pm – 2:40 pm BREAK

2:40 pm – 3:40 pm

Empire Ballroom Session 3A: **GOING AFTER DEFECTS**
Moderator: J. Figueras – Univ. Poli Catalunya

3A.1 *On a New Outlier Rejection Technique,* C. Thibeault – Ecole Tech. Sup. Montreal

3A.2 *Enhanced Resolution Jitter Testing Using Jitter Expansion,* H. Choi, D. Han, A. Chatterjee – Georgia Inst. of Technology

3A.3 *Using Clock-Vdd to Test and Diagnose the Power-Switch in Power-Gating Circuit,* H.-H. Huang, C.-H. Cheng – Feng-Chia Univ.

2:40 pm – 3:40 pm

Napa 1, 2, 3 Session 3B: **ONLINE TEST**
Moderator: M. Nicolaidis – TIMA Labs

3B.1 *A Programmable Window Comparator for Analog Online Testing,* A. Laknaur, R. Xiao, H. Wang – Southern Illinois Univ.

3B.2 *Probabilistic Compensation for Digital Filters Under Pervasive Noise-Induced Operator Errors,* M. Ashouei, A. Chatterjee, S. Bhattacharya – Georgia Inst. of Technology

3B.3 *Error Tolerance in DNA Self-Assembly by (2k-1X) x (2k-1) Snake Tile Sets,* X. Ma, J. Huang, F. Lombardi – Northeastern Univ.

2:40 pm – 3:40 pm

Sonoma Session 3C: **SYSTEM TEST AND NTFS**
Organizer/Moderator:
S. Mitra – Stanford Univ.

3C.1 *Debugging Returns: Use All the Information You Possess,* S. Davidson – Sun Microsystems

3C.2 *Correlating Test Data From System Test to ATE,* Z. Conroy – Cisco

3C.3 *System Test and NTFS*, B. Eklow – Cisco

3:40 pm – 4:00 pm BREAK

4:00 pm – 5:00 pm

Empire Ballroom Session 4A: **DIAGNOSIS I**
Moderator: C. Landrault – LIRMM

4A.1 *Diagnosis of Bridging Defects Based On Current Signatures at Low Power Supply Voltages,* D. Arumi, R. Rodriguez-Montanes, J. Figueras – Univ. Politècnica De Catalunya; S. Eichenberger, C. Hora, B. Kruseman, M. Lousberg, A.K. Majhi – NXP Semiconductors

4A.2 *Handling Pattern-Dependent Delay Faults in Diagnosis,* J.-W. Chen, Y.-Y. Chen, J.-J. Liou – Natl. Tsing Hua Univ.

4A.3 *Diagnosis of Full Open Defects in Interconnecting Lines,* R. Rodriguez-Montanes, D. Arumí, J. Figueras – Univ. Politècnica De Catalunya, S. Eichenberger, C. Hora, B. Kruseman, M. Lousberg, A.K. Majhi – NXP Semiconductors

4:00 pm – 5:00 pm

Napa 1, 2, 3 Session 4B: **ATPG FOR DELAY FAULTS**
Moderator: F. Lombardi – Northeastern Univ.

4B.1 *Glitch-Aware Pattern Generation and Optimization Framework for Power-Safe Scan Test,* V.R. Devanathan, C.P. Ravikumar – Texas Instruments; V. Kamakoti – Indian Institute of Technology, Madras

4B.2 *An Integrated Framework for At-Speed and ATE-Driven Delay Test of Contract-Manufactured ASICs,* V. Iyengar, K. Pichamuthu, A. Ferko, F. Woytowich, D. Lackey, G. Grise, M. Taylor, M. Degregorio, S. Oakland – IBM

4B.3 *Supply Voltage Noise Aware ATPG for Transition Delay Faults,* N. Ahmed, M. Tehranipoor – Univ. of Connecticut; V. Jayaram – Texas Instruments

4:00 pm – 5:00 pm

Sonoma

Session 4C: **HIGH-SPEED TEST**
Organizer/Moderator:
S. Tabatabaei – Guide Technology

4C.1 *Injecting Jitter to Measure Jitter: A Production Test Methodology for Gbps Transceivers,* M. Hafed - DFT Microsystems

4C.2 *Challenges and Practices in High Speed Interface Testing,* S. Abdennadher - Intel

4C.3 *An ATE Approach to At-Speed Functional and Jitter Test of High Speed Serial Buses,* S. Munroe - Teradyne

8:00 pm – 9:30 pm

Empire Ballroom

Session 5A – EMBEDDED TUTORIAL:
STATISTICAL AND DATA MINING METHODS FOR TEST-BASED YIELD LEARNING
Organizer: D. Appello – STMicroelectronics
Moderator: S. Tragoudas – Southern Illinois Univ.
Co-Organized with:

5A.1 *Scan Diagnostics for Yield Learning,* C. Hay – Synopsys

5A.2 *Embedded Memory Diagnosis and Yield Acceleration,* G. Torjian, Y. Zorian – Virage Logic

5A.3 *Analysis of Diagnostic Data from Test Chips and Production Devices,* A. Adamov – Synopsys

8:00 pm – 9:30 pm

Napa 1, 2, 3

Session 5B – PANEL: **CONVERSATIONS WITH TEST EXPERTS**
Organizer: R. Kapur – Synopsys
Moderator: E.J. McCluskey – Stanford Univ.
Panelists:
A. Gattiker – IBM
S. Mitra – Stanford Univ.
T.W. Williams – Synopsys

25th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Tuesday, May 8th, 2007

7:30 am – 8:30 am Registration, Continental Breakfast

8:30 am – 9:30 am

Empire Ballroom Session 6A: **ADVANCES IN TEST**
Moderator: R. Makki – UAE Univ.

6A.1 *Test Set Reordering Using the Gate Exhaustive Test Metric,* K.Y. Cho, E.J. McCluskey – Stanford Univ.

6A.2 *An Analysis of Defect Detection for Weighted Random Patterns Generated with Observation/ Excitation-Aware Partial Fault Targeting,* J. Dworak – Brown Univ.

6A.3 *Using Multiple Expansion Ratios and Dependency Analysis to Improve Test Compression,* R. Putman – Cirrus Logic; N.A. Touba – Univ. of Texas Austin

8:30 am – 9:30 am

Napa 1, 2, 3 Session 6B: **DIAGNOSIS II**
Moderator: L. Anghel – TIMA Labs

6B.1 *Accelerating Diagnosis via Dominance Relations Between Sets of Faults,* R. Adapa, S. Tragoudas – Southern Illinois Univ.; M. Michael – Univ. of Cyprus

6B.2 *Speeding Up Effect-Cause Defect Diagnosis Using a Small Dictionary,* W. Zou, W.-T. Cheng, H. Tang – Mentor Graphics; S.M. Reddy – Univ. of Iowa

6B.3 *Using Scan-Dump Values to Improve Functional-Diagnosis Methodology,* V.C. Vimjam, M. Hsiao – Virginia Tech; M.E. Amyeen, S. Venkataraman – Intel; R. Guo – Mentor Graphics; K. Yang – Novas Software

8:30 am – 9:30 am

Sonoma Session 6C: **TESTING ALONE ISN'T ENOUGH: RELIABILITY CHALLENGES IN SCALED CMOS**
Organizer/Moderator: P. Sanda – IBM

6C.1 *Reliability Challenges of Scaled CMOS,* J. Maiz – Intel

6C.2 *Challenges of Burn-In and Impact to Test,* P. Nigh – IBM

6C.3 *Case Study of Designing a Reliable System With Reliability Failures and Soft Errors in Mind,* D. Abts – Cray

25th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Tuesday, May 8th, 2007

9:30 am – 9:50 am BREAK

9:50 am – 10:50 am

Empire Ballroom

Session 7A: **FAILURE ESTIMATION**
Moderator: A. Chatterjee – Georgia Inst. of Technology

7A.1 *A UML Based System Level Failure Rate Assessment Technique for SoC Designs,* M. Hosseinabady, M.H. Neishaburi, P. Lotfi-Kamran – CAD Research Group, Univ. of Tehran; Z. Navabi – Northeastern Univ.

7A.2 *An Analysis Framework for Transient-Error Tolerance,* J.P. Hayes – Univ. of Michigan; I. Polian, B. Becker – Albert-Ludwigs Univ.

7A.3 *Case Study: Soft Error Rate Analysis in Storage Systems,* B. Mullins, H. Asadi, M.B. Tahoori, D. Kaeli – Northeastern Univ.; K. Granlund, R. Bauer, S. Romano – EMC

9:50 am – 10:50 am

Napa 1, 2, 3

Session 7B: **FAULT PREDICTION & EVALUATION**
Moderator: Z. Navabi – Univ. of Tehran

7B.1 *Silicon Evaluation of Static Alternative Fault Models,* C. Schuermyer, J. Pangilinan – LSI Logic; J. Jahangiri, M. Keim, J. Rajski, B. Benware – Mentor Graphics

7B.2 *Parameter Estimation for a Model with Both Imperfect Test and Repair,* S. Wilson, B. Flood – Trinity College Dublin; S. Goyal, S. Bergin – Bell Labs Ireland; J. Mosher, J. O'Brien, R. Kennedy – Lucent Technologies

7B.3 *Circuit Failure Prediction and Its Application to Transistor Aging,* M. Agarwal, S. Mitra – Stanford Univ.; B.C. Paul – Toshiba; M. Zhang – Intel

9:50 am – 10:50 am

Sonoma

Session 7C: **OPEN AND HIGHLY EXTENDABLE YIELD DIAGNOSTICS SOLUTIONS**
Organizer: T. Jackson – Cadence
Moderator: K. Hatayama – STARC

7C.1 *Early Life Cycle Yield Improvement of Nanometer Chips Using Volume Yield Diagnostics Analysis,* S. Seike, K. Namura, Y. Ohya – IBM Japan Services

7C.2 *Expanding Role of ATE: From Quality Screens to Yield Metrology,* A. Khoche – Verigy

7C.3 *Impacts of a Volume Mode Yield Diagnostics System,* T. Jackson, D. Meehl, A. Uzzaman – Cadence

10:50 am – 11:10 am BREAK

11:10 am – 12:10 pm

Empire Ballroom Session 8A: **ANALOG TEST**
Moderator: R. Pendurkar – Sun

8A.1 *Transformer-Coupled Loopback Test for Differential Mixed-Signal Specifications,* B. Kim, J.A. Abraham – Univ. of Texas Austin; Z. Fu – National Semiconductor

8A.2 *Novel Cross-Loopback Based Test Approach for Specification Test of Multi-Band, Multi-Hardware Radios,* V. Natarajan, G. Srinivasan, A. Chatterjee – Georgia Inst. of Technology; C. Force – Texas Instruments

8A.3 *Code-Density Test of Analog-to-Digital Converters Using Single Low-Linearity Stimulus Signal,* L. Jin – National Semiconductor; D. Chen, R. Geiger – Iowa State Univ.

11:10 am – 12:10 pm

Napa 1, 2, 3 Session 8B: **HIGH LEVEL TEST TECHNIQUES**
Moderator: C. Metra – Univ. of Bologna

8B.1 *High Level Synthesis of Degradable ASICS Using Virtual Binding,* N. Honarmand, A. Shahabi, H. Sohofi, Z. Navabi – Univ. of Tehran; M. Abbaspur – Shahid Beheshti Univ.

8B.2 *Efficient RTL Coverage Metric for Functional Test Selection,* J. Kang, S.C. Seth – Univ. of Nebraska; V. Gangaram – Intel

8B.3 *RTL Test Point Insertion to Reduce Delay Test Volume,* K.J. Balakrishnan – AMD; L. Fang – Virginia Tech

11:10 am – 12:10 pm

Sonoma Session 8C: **IMPACT OF NEW MEMORY FAILURE MODES**
Organizer/Moderator:
A. Yessayan – Virage Logic

8C.1 *Memory Failure Modes and Tests in Embedded DRAM,* S. Kengeri – TSMC

8C.2 *Dealing With New Memory Failure Modes in Today's Complex SoCs,* Y. Zorian – Virage Logic

8C.3 *Impact of SOI Technology on Memory Failure Modes,* M. D'abreu – AMD

12:10 pm – 1:45 pm LUNCH

1:45 pm – 3:15 pm

Empire Ballroom

Session 9A – HOT TOPIC SESSION: **FAULT TOLERANT NANOSCALE ARCHITECTURES — THE CHALLENGES AND EMERGING SOLUTIONS**
Organizer: A. Ivanov – Univ. of British Columbia
Moderator: P. Pande – Washington State Univ.
Presenters:
A. DeHon – Univ. of Pennsylvania
F. Lombardi – Northeastern Univ.
M. Stan – Univ. of Virginia

1:45 pm – 3:15 pm

Napa 1, 2, 3

Session 9B – SPECIAL SESSION: **TTTC 2007 BEST DOCTORAL THESIS AWARD**
Organizer: A. Veneris – Univ. of Toronto
Moderator: Y. Makris – Yale Univ.

1:45 pm – 3:15 pm

Sonoma

Session 9C – HOT TOPIC SESSION: **MAKING ANALOG & MIXED SIGNAL TESTING AS ROBUST AS DIGITAL**
Organizer: D.M. Wu – Intel
Moderator: A. Veneris – Univ. of Toronto
Presenters:
A. Chatterjee – Georgia Inst. of Technology
G. Roberts – McGill Univ.
D.M. Wu – Intel
Invited Experts:
M. Soma – Univ. of Washington
G. Taylor – Intel

3:30 pm – 11:00 pm

SOCIAL PROGRAM
See page 29 for more information.

25th IEEE VLSI TEST SYMPOSIUM
TECHNICAL PROGRAM
Wednesday, May 9th, 2007

8:00 am – 9:00 am Registration, Continental Breakfast

9:00 am – 10:00 am

Empire Ballroom Session 10A: **MEMORY REPAIR**
Moderator: B. Wang – AMD

10A.1 *Multiple Bit Upset Tolerant Memory Using a Selective Cycle Avoidance Based SEC-DED-DAEC Code,* A. Dutta. N.A. Touba – Univ. of Texas Austin

10A.2 *A Built-In Self-Repair Scheme for Multiport RAMs,* T.-W. Tseng, C.-H. Wu, Y.-J. Huang, J.-F. Li – Natl. Central Univ.; A. Pao, K. Chiu, E. Chen – Faraday Tech. Corporation

10A.3 *Un-Restored Destructive Write Faults Due to Resistive-Open Defects in the Write Driver of SRAMS,* A. Ney, P. Girard, C. Landrault, S. Pravossoudovitch, A. Virazel – LIRMM; M. Bastian – Infineon

9:00 am – 10:00 am

Napa 1, 2, 3 Session 10B: **SOC TEST**
Moderator: L. Milor – Georgia Inst. of Technology

10B.1 *Using Domain Partitioning in Wrapper Design for IP Cores Under Power Constraints,* T.E. Yu, T. Yoneda, H. Fujiwara – Nara Inst. of Science and Technology; D. Zhao – Univ. of Louisiana Lafayette

10B.2 *Design of Test Access Mechanism for AMBA-Based System-on-a-Chip,* S. Park, J. Song, P. Min, H. Yi – Hanyang Univ.

10B.3 *TAM Design and Optimization for Transparency-Based SoC Test,* T. Yoneda, H. Fujiwara – Nara Inst. of Science and Technology; A. Shuto – Sony Semiconductor Kyushu Co., Ltd.; H. Ichihara, T. Inoue – Hiroshima City Univ.

10:00 am – 10:20 am BREAK

10:20 am – 11:20 am

Empire Ballroom Session 11A: **RF TEST II**
Moderator: C.H. Chiang – Lucent Technologies

11A.1 *A Low Cost Spectral Power Extraction Technique for RF Transceiver Testing,* T.-L. Hung, J.-L. Huang – Natl. Taiwan Univ.

11A.2 *Alternate Diagnostic Testing and Compensation of RF Transmitter Performance Using Response Detection,* R. Senguttuvan; A. Chatterjee – Georgia Inst. of Technology

11A.3 *A Low-Noise Amplifier with Integrated Current and Power Sensors for RF BIST Applications,* Y.-C. Huang, H.-H. Hsieh, L.-H. Lu – Natl. Taiwan Univ.

10:20 am – 11:20 am

Napa 1, 2, 3 Session 11B: **DESIGN FOR TEST**
Moderator: H. ElTahawy – Mentor Graphics

11B.1 *Automated Design and Insertion of Optimal One-Hot Bus Encoders,* P. Wohl, J.A. Waicukauski, S. Patel – Synopsys

11B.2 *Autoscan-Invert: An Improved Scan Design Without External Scan Inputs or Outputs,* I. Pomeranz – Purdue Univ.; S.M. Reddy – Univ. of Iowa

11B.3 *Transition Fault Testability in Bit Parallel Multipliers Over GF (2m),* H. Rahaman, B.K. Sikdar – Bengal Eng. and Science Univ.; J. Mathew, D.K. Pradhan – Univ. of Bristol

10:20 am – 11:20 am

Sonoma Session 11C: **COLLABORATIVE DFT PRACTICES NEEDED FOR LOW-COST TESTING**
Organizers: S. Ravi – Texas Instruments
C.P. Ravikumar – Texas Instruments
Moderator: C.P. Ravikumar – Texas Instruments

11C.1 *Influencing Test of Complex SoCs Through Generic DFT,* S. Kale, S.K. Vooka, R.A. Parekhji – Texas Instruments

11C.2 *Innovative DFT Flows for "Pushing-the-Envelope" Designs,* M. Hussain, S. Krishnamurthi – Synopsys; C.P. Ravikumar – Texas Instruments

11C.3 *Providing Value Add Manufacturing Test Solutions,* S. Chinamilli, Y. Senthilkumar, R. Vaddempudi – Tessolve

11:20 am – 11:40 am BREAK

11:40 am – 12:40 pm

Empire Ballroom Session 12A: **TESTING LARGE CHIPS**
Moderator: K. Ruparel

12A.1 *DfT for the Reuse of Networks-On-Chip as Test Access Mechanism,* A.M. Amory, M. Lubaszewski – UFRGS; F. Ferlini, F. Moraes – PUCRS

12A.2 *Novel Approach to Clock Fault Testing for High Performance Microprocessors,* C. Metra, M. Omana – Univ. of Bologna; T.M. Mak, S. Tam – Intel

12A.3 *At-Speed Testing of Core-Based System-On-Chip Using an Embedded Micro-Tester,* M. Tuna, M. Benabdenbi, A. Greiner – UPMC Paris VI

11:40 am – 12:40 pm

Napa 1, 2, 3 Session 12B: **ENSURING SECURE CHIPS**
Moderator: E. Volkerink – Verigy

12B.1 *VIm-Scan: A Low Overhead Scan Design Approach for Protection of Secret Key in Scan-Based Secure Chips,* S. Paul, R. Chakraborty, S. Bhunia – Case Western Reserve Univ.

12B.2 *Effects of Embedded Decompression and Compaction Architectures on Side-Channel Attack Resistance,* C. Liu – Univ. of Nebraska-Lincoln; Y. Huang – Mentor Graphics

11:40 am – 12:40 pm

Sonoma Session 12C: **BOARD AND SYSTEM LEVEL MEMORY CLUSTER TEST PROBLEMS AND PROPOSED SOLUTIONS**
Organizer: H. Ehrenberg – GOEPEL Electronics
Moderator: R. Kapur – Synopsys

12C.1 *State of the Art in Memory Cluster Testing at Board and System Level,* H. Ehrenberg – GOEPEL Electronics; R. Sowada – Honeywell

12C.2 *Challenges Related to Memory Cluster Tests,* R. Sowada - Honeywell

12C.3 *P1581 - New Possibilities for Static Component Interconnect Test,* S. Creekpaum – ASSET InterTech

12:40 pm – 2:00 pm LUNCH

2:00 pm – 3:30 pm

Empire Ballroom Session 13A – NEW TOPIC SESSION: **NANO-ELECTRONICS WILL BE ASYNCHRONOUS**
Organizer: B. Courtois – TIMA Labs
Moderator: P. Maxwell – Micron
Presenter:
A.J. Martin – Caltech

2:00 pm – 3:30 pm

Napa 1, 2, 3

Session 13B – HOT TOPIC SESSION:
TESTING IN THE PRESENCE OF NOCS
Organizers: E.J. Marinissen – NXP Semiconductors
N. Nicolici – McMaster Univ.
Moderator: N. Nicolici – McMaster Univ.
Presenters:
E. Cota – UFRGS
A. Ivanov – Univ. of British Columbia
E.J. Marinissen – NXP Semiconductors

2:00 pm – 3:30 pm

Sonoma

Session 13C – PANEL: **RF YIELD: IS IT A PROBLEM?**
Organizers: A. Khoche – Verigy
M. Slamani – IBM Microelectronics
Moderator: C. Force – Texas Instruments
Panelists:
M. Berry – Amkor
J. Hjort – IBM
D.A. Pollek – ChipMP
G. Verma – Qualcomm
S. Zanella – PDF Solutions

TEST TECHNOLOGY EDUCATIONAL PROGRAM 2007

The Tutorials and Education Group of TTTC continues for an 8th year the organization of a comprehensive set of test technology tutorials. These comprise tutorials in conjunction with TTTC-sponsored technical meetings, web-based tutorials, and on-site tutorials and courses. The tutorials are part of the successful annual Test Technology Educational Program (TTEP 2007).

TTEP intends to serve both test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics and also the opportunity to earn official certification from IEEE TTTC. Each six-hour tutorial corresponds to four TTEP units. Upon completion of each sixteen TTEP units official accreditation in the form of an "IEEE TTTC Test Technology Certificate" is presented to the participants.

The Test Technology Educational Program 2007 includes (but is not limited to) tutorial units presented in conjunction with the the following TTTC sponsored technical meetings (in chronological order):

- Latin American Test Workshop (LATW'07), March 11–14, Cuzco, Peru
- Design Automation & Test in Europe Conference (DATE'07), April 16–20, Nice, France
- VLSI Test Symposium (VTS'07), May 6–10, Berkeley, California, USA
- Signal Propagation on Interconnects Workshop (SPI'07), May 13–16, Portofino, Italy
- European Test Symposium (ETS'07), May 20–24, Freiburg, Germany
- International On-Line Testing Symposium (IOLTS'07), July 2–4, Crete, Greece
- Asian Test Symposium (ATS'07), October 9–11, Beijing, China
- International Test Conference (ITC'07), October 22–26, Santa Clara, California, USA

For further information contact:

Dimitris Gizopoulos - Tutorials and Education Group Chair
Univ. of Piraeus – Greece
Tel: +30-210-414-2372
E-mail: *dgizop@unipi.gr*

For a detailed list of tutorials and tutorial descriptions, visit the TTEP website:

http://tab.computer.org/tttc/teg/ttep

Sunday, May 6th, 2007
TUTORIALS

The 2007 VLSI Test Symposium includes three excellent TTEP 2007 tutorials on high interest test technology topics. All three tutorials qualify for IEEE TTTC certification. One tutorial will be presented on Sunday, May 6th and two on Thursday, May 10th. Each tutorial requires a separate fee and registration (see General Information, page 6).

7:30 am – 8:30 am Tutorial Registration, Continental Breakfast

8:30 am – 4:30 pm
Lanai 2 TUTORIAL 1: **SCAN DELAY TESTING OF NANOMETER SOCS**

Presenter:
A. Singh – Auburn Univ.

AUDIENCE: VLSI Design and Test engineers and researchers, engineering managers, and also reliability engineers and managers.

DESCRIPTION: Delay defects that degrade performance and cause timing-related failures are emerging as a major problem in nanometer technologies. Structural scan-based delay testing is being pursued as a possible cost effective solution for this problem. However, recent research indicates that several formidable challenges must be overcome before it can become fully effective. These include poor coverage of launch-on-capture scan test, and also that the observed signal timing may not reflect true circuit delays in normal functional operation due to false paths, power supply noise, clock stretching, etc. This tutorial aims at a comprehensive discussion of these challenges, along with proposed solutions, mainly aided by data from industrial studies.

Thursday, May 10th, 2007
TUTORIALS

7:30 am – 8:30 am Tutorial Registration, Continental Breakfast

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8:30 am – 4:30 pm
Lanai 2 TUTORIAL 2: **: DEALING WITH TIMING ISSUES FOR SUB-100N DESIGNS – FROM MODELING TO MASS PRODUCTION**
Presenters:
L.-C. Wang – UC Santa Barbara
M. Abadir – Freescale

AUDIENCE: Test and debug engineers, researchers, and tool developers who are interested in understanding the impacts of sub-100n manufacturing processes on timing and in learning how to model them, analyze them, and deal with them at various stages of design, from library development to silicon test and debug.

DESCRIPTION: This tutorial intends to give attendees an overall picture on timing issues induced by process variations with sub-100n manufacturing processes. The issues can be divided into three parts: (1) modeling, (2) analysis, and (3) test and debug. In the modeling part, the tutorial covers the issues of statistical process characterization. It discusses how variation models are characterized with test structures and how these models can be used to in analyzing timing. Then, timing analysis and statistical timing analysis are discussed. How timing problems are debugged on silicon and how to devise a reliable speed binning strategy is then covered. Industrial results are discussed on correlating functional tests to structural tests in speed binning as well as experiments on correlating delay test results back to timing analysis results. This tutorial emphasizes the connections between pre-silicon modeling and analysis and post-silicon test and debug methodologies.

8:30 am – 4:30 pm
Lanai 3 TUTORIAL 3: **DFX: THE CONVERGENCE OF YIELD, MANUFACTURING, AND TEST**
Presenter: R. Aitken – ARM

AUDIENCE: Test practitioners (engineers, students, academics) who are interested in learning more about the interaction between design and test as they relate to yield, manufacturability, and variability, and how they will affect chips in sub-90nm process technology.

DESCRIPTION: The tutorial goal is to show how Design For Yield (DFY) and Design For Manufacturability (DFM) are tightly coupled into what we conventionally think of as test, and that as process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of test-limited yield, yet this concept is common in DFT (e.g. I_{DDQ} testing, delay testing). This tutorial provides the background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conduct their own research in the area, and to apply these concepts in their jobs.

IEEE Workshop on
Test of Wireless Circuits and Systems

WTW 2007

May 6th, 2007

SCOPE: The Wireless Test Workshop (WTW) includes, among others, the following major topics in RF test: Case Studies, High-Frequency Test, Embedded RF Circuit Test, RF Test Board Related Issues, Yield Learning, Wireless Test Methodology, Standards Conformance Test, Noise Characterization and Validation, Economics of Test, Wireless Product Test Equipment and Metrology.

For this year, the program committee has put together an exciting and a highly technical program that includes: an invited speaker, Craig Force of Texas Instruments, 1 mini-tutorial on 3G standards, plus 10 other technical papers. The workshop encourages discussion and the technical program is oriented to create an atmosphere that facilitates audience learning and contribution to the subject matter.

Advance Program Summary:

1) Invited Speaker:	Advanced Wireless Technology and the Next Billion Users
2) Session #1:	RF Test Instruments
3) Session #2:	Mini-Tutorial: DIGRF 3G Cell Phone Standard
4) Session #3:	WIMAX & Test Challenges
5) Session #4:	RF Test Techniques and Standards I
6) Session #5:	RF Test Techniques and Standards II

REGISTRATION: All WTW 2007 participants require registration, which includes workshop technical sessions, workshop informal proceedings, break refreshments, and lunch.

SPONSORSHIP: WTW 2007 is sponsored by the IEEE Computer Society TTTC.

INFORMATION: For further details on the technical program, please contact Program Chair, Mustapha Slamani (*slamanim@us.ibm.com*). Regarding other questions, please contact the General Chair, Rob Aitken (*rob.aitken@arm.com*).

Please visit our web-site:

http://www.wtw2007.tec.ufl.edu/

IEEE International Workshop on Open Source Test Technology Tools

IOST3 2007

May 9th-10th, 2007

The IOST3 workshop supports a community of practice focused on open source and open interface tools for test, quality assurance, and reliability estimation of electronic devices, assemblies, and systems.

Unique among workshops, IOST3 delivers to its attendees immediately useful tools and libraries, as well as new thoughts and ideas in the rapidly evolving world of test technology.

This year's workshop will focus on data management – test vector standards, datalogs, validation and analytical tools, and particularly on the aggregation and correlation of data from disparate sources that effective collaboration can provide. Design data for IC's, subassemblies, and systems, failure and repair reports, and production equipment histories all play a role in identifying root causes and improving reliability. The warp and woof of collaboration and competition create the fabric of civilization's progress, and the open source milieu has been found to provide a dramatic new means to facilitate that progress. IOST3 is exploring that milieu for the benefit of semiconductor and system test in a worldwide community.

In-depth presentations from technical experts from such technology leaders as IBM, Sun, Cisco, and Verigy, and such academic powerhouses as Politecnico di Torino in Italy and Stanford in California, together with innovative newcomers with exciting and novel advances, provide a rich and stimulating opportunity to interact with colleagues who share your interests.

http://www.iost3.org/

SOCIAL PROGRAM
Tuesday, May 8th, 2007

This year's Social Event will provide a relaxing atmosphere for networking and socializing, as well as an evening of entertainment.

From The Claremont Hotel in Berkeley, we will travel via luxury motor coach to one of the East Bay's oldest parks in the District, the jewel of the system: Tilden Park. Tilden Park will offer two attractions for our group: the Botanic Garden and Lake Anza. The Botanic Garden contains the world's most complete collection of California native plants, including rare and endangered species. There will be two guided tours of the Botanic Garden starting at 4:00 pm and 5:00 pm. While some enjoy the Botanic Garden, others will enjoy the sun and sand at Lake Anza, a favorite Berkeley getaway. Its sandy beach is open to the sun and sheltered from the wind.

The evening will continue at *Hs Lordships Restaurant*, where we will enjoy a sumptuous meal with panoramic views and a sunset on the Bay. Our entertainment for the evening is You, with DJ/ Karaoke host Amy Foster, as featured at our 2004 VTS Social Event on the Hornblower Cruise. Music, singing, and dancing will round out our evening and promise to provide memories for all.

IEEE
Design & Test of Computers

IEEE D&T is a bimonthly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers, and researchers. D&T features peer-reviewed original work describing methods and practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

- System Level Design and Test
- Embedded Test Technology
- Low Power Design
- Reconfigurable Systems
- Board and System Test
- Analog and Mixed Signal Design and Test
- System-on-Chip Design and IP Reuse
- Embedded Systems and Software
- Design and Verification/Validation

In addition, D&T publishes tutorial articles, perspectives, roundtable discussions, book reviews, viewpoints, conference reports, panel summaries, and standards updates contributed by authors working in the industry.

PAPER SUBMISSION: Authors should use *Manuscript Central* (https://mc.manuscriptcentral.com/cs-ieee) to upload their submissions. The first-time user must create a new account. The site provides detailed instructions on usage. Each submitted paper undergoes at least three technical reviews. All submissions must be original, previously unpublished work.

SPECIAL ISSUES: The theme issues for 2007 are (please check D&T website for submission instructions and deadlines):

Jan/Feb	Biochips
March/April	Advances in Functional Validation through Hybrid Techniques
May/June	IR-Drop and Power Supply Noise Effects on Design and Test
July/August	Special Section on CAD for Emerging Technologies
Sep/Oct	Globally Asynchronous and Locally Synchronous Design and Test
Nov/Dec	Design and Test of ICs for Secure Embedded Computing

SUBSCRIPTION: IEEE D&T offers full year and half-year subscriptions for print issues. In addition, it offers to IEEE CS and CAS members electronic subscription options with full text searchable access to all issues from 1995 forward!

Anyone may access tables of content and abstracts of articles online at no cost, so check out D&T's web page at:

http://computer.org/dt

IEEE Design&Test of Computers

25th IEEE VLSI Test Symposium (VTS 2007)

Sunday, May 6th, 2007

7:30 am – 8:30 am	TUTORIAL/WORKSHOP REGISTRATION	
8:30 am – 4:30 pm	WORKSHOP: WTW 2007 *(8:30 am – 5:30 pm)*	Tutorial 1: Scan Delay Testing of Nanometer SoCs

Monday, May 7th, 2007

7:30 am – 9:00 am	REGISTRATION		
9:00 am – 10:30 am	PLENARY SESSION		
11:00 am – 12:00 pm	Session 1A: RF Testing I	Session 1B: Delay Test Quality	Session 1C: Design in the Presence of Variations: Characterization, Monitoring, and Response
1:20 pm – 2:20 pm	Session 2A: Memory Test	Session 2B: Test Compression	Session 2C: Small Delay Test in Practice
2:40 pm – 3:40 pm	Session 3A: Going After Defects	Session 3B: Online Test	Session 3C: System Test and NTFS
4:00 pm – 5:00 pm	Session 4A: Diagnosis I	Session 4B: ATPG for Delay Faults	Session 4C: High-Speed Test
8:00 pm – 9:30 pm	Session 5A - Embedded Tutorial: Statistical and Data Mining Methods for Test-Based Yield Learning	Session 5B - Panel: Conversations with Test Experts	

Tuesday, May 8th, 2007

7:30 am - 8:30 am	REGISTRATION		
8:30 am – 9:30 am	Session 6A: Advances in Test	Session 6B: Diagnosis II	Session 6C: Testing Alone Isn't Enough: Reliability Challenges in Scaled CMOS
9:50 am - 10:50 am	Session 7A: Failure Estimation	Session 7B: Fault Prediction & Evaluation	Session 7C: Open and Highly Extendable Yield Diagnostics Solutions

11:10 am – 12:10 pm	Session 8A: Analog Test	Session 8B: High Level Test Techniques	Session 8C: Impact of New Memory Failure Modes
1:45 pm – 3:15 pm	Session 9A - Hot Topic Session: Fault Tolerant Nanoscale Architectures — the Challenges and Emerging Solutions	Session 9B - Special Session: TTTC 2007 Best Doctoral Thesis Award	Session 9C - Hot Topic Session: Making Analog & Mixed Signal Testing as Robust as Digital

Wednesday, May 9th, 2007

7:30 am - 9:00 am	REGISTRATION		
9:00 am – 10:00 am	Session 10A: Memory Repair	Session 10B: SoC Test	
10:20 am – 11:20 am	Session 11A: RF Test II	Session 11B: Design for Test	Session 11C: Collaborative DFT Practices Needed for Low-Cost Testing
11:40 am – 12:40 pm	Session 12A: Testing Large Chips	Session 12B: Ensuring Secure Chips	Session 12C: Board and System Level Memory Cluster Test Problems and Proposed Solutions
2:00 pm – 3:30 pm	Session 13A - New Topic Session: Nano-Electronics Will be Asynchronous	Session 13B - Hot Topic Session: Testing in the Presence of NoCs	Session 13C - Panel: RF Yield: Is It a Problem?
4:00 pm - 6:00 pm	WORKSHOP: IOST3 2007		

Thursday, May 10th, 2007

7:30 am – 8:30 am	TUTORIAL REGISTRATION	
8:30 am - 4:30 pm	Tutorial 2: Dealing with Timing Issues for Sub-100n Designs – From Modeling to Mass Production	Tutorial 3: DFX: The Convergence of Yield, Manufacturing, and Test
8:00 am - 5:30 pm	WORKSHOP: IOST3 2007	

- Innovative Practices Session *- Special Session*

25th IEEE VLSI Test Symposium (VTS 2007)
FRINGE TECHNICAL MEETINGS

A number of TTTC professional groups interested in test will hold their meetings at VTS 2007. At press time, the following meetings were scheduled. These meetings are for members. If you'd like to attend, please contact the person listed at the e-mail address given.

MONDAY, May 7th

*12:00 pm - 1:20 pm — **Test Week Workshop Coordination**
Yervant Zorian (*zorian@viragelogic.com*)

2:00 pm - 3:00 pm — **TTTC Executive Committee**
Andre Ivanov (*ivanov@ece.ubc.ca*)

3:00 pm - 4:00 pm — **TTTC Tutorials and Education Group**
Dimitris Gizopoulos (*dgizop@unipi.gr*)

6:00 pm - 8:00 pm — **IEEE VTS Program Committee**
Alex Orailoglu (*alex@cs.ucsd.edu*)

TUESDAY, May 8th

8:00 am - 9:30 am — **TTTC Technical Meetings Review Committee**
Chen-Huan Chiang (*chenhuan@lucent.com*)

*12:10 pm - 1:45 pm — **TTTC Middle East and Africa Group**
Rafic Makki (*makki@uaeu.ac.ae*)

*12:10 pm - 1:45 pm — **IEEE IOLTS Program Committee**
Michael Nicolaidis (*michael.nicolaidis@imag.fr*)
Dimitris Gizopoulos (*dgizop@unipi.gr*)
T. M. Mak (*t.m.mak@intel.com*)

*12:10 pm - 1:45 pm — **IEEE DBT Planning Committee**
Jim Plusquellic (*plusquel@csee.umbc.edu*)

2:00 pm - 3:00 pm — **TTTC Communications Group**
Adit Singh (*adsingh@eng.auburn.edu*)

WEDNESDAY, May 9th

8:00 am - 9:30 am — **TTTC Operations Committee**
Andre Ivanov (*ivanov@ece.ubc.ca*)

10:00 am - 12:00 pm — **IEEE VTS Organizing Committee**
Paolo Prinetto (*paolo.prinetto@polito.it*)

**Meeting During Lunch Break*